ME-8440

AUSTRON MODEL 2100 LORAN-C TIMING RECEIVER OPERATION AND MAINTENANCE MANUAL

AUSTRON

AUSTRON INC. 1915 KRAMER LANE, AUSTIN, TEXAS 78758 (512) 836-3523 TWX 910/874-1356

ME-8440

AUSTRON MODEL 2100 LORAN-C
TIMING RECEIVER
OPERATION AND MAINTENANCE MANUAL

October, 1981

P/N 12798096

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case, the user at his own expense will be required to take whatever measures may be required to correct the interference.

WARRANTY

AUSTRON, INC., of Austin, Texas, warrants, for one year after delivery, to the original purchaser of any product manufactured by AUSTRON, that same shall be free of defects in material and workmanship. Obligation under this warranty shall be limited to repair or replacement, at AUSTRON's discretion, of any product or part thereof which has been returned by the original purchaser with transportation prepaid, and upon examination by AUSTRON, is found to be defective. AUSTRON assumes no responsibility for loss or damage to equipment being returned for repair or replacement under the terms of this warranty.

For this warranty to be effective, the purchaser agrees that the equipment will be properly installed and maintained. Equipment which, upon examination by AUSTRON, requires repair or replacement of parts thereof as a result of improper installation, misuse, unauthorized alterations or repairs, or user negligence, such repairs or replacement of parts thereof will be made at cost.

AUSTRON makes no representation or warranty of any kind, either expressed or implied, with respect to equipment operation and procedures. Any action that the user may take in reliance upon the operation or accuracy of this equipment shall be taken solely upon the user's own responsibility and risk.

AUSTRON shall not be liable for consequential damages to purchaser, user, or any others resulting from the possession or use of this equipment.

Prior to return of a product under terms of this warranty, AUSTRON, INC., Austin, Texas, is to be notified. Notification is to include the Model Number and Serial Number of the product and full details of the problem.

MODEL 2100 LORAN-C TIMING RECEIVER

INTRODUCTION

This manual is written for personnel operating or maintaining the Model 2100 Loran-C Timing Receiver, manufactured by AUSTRON, INC.

This manual contains information about the physical and electrical specifications, installation and preliminary adjustment procedures, operating steps, functional analysis and precise access descriptions, parts lists, PCB assembly drawings, and other applicable drawings and diagrams required to adequately support the equipment.

AMENDMENT
NOTICE

AUSTRON, INC., makes every attempt to provide up-to-date manuals with the associated equipment. Occasionally, changes are made to equipment wherein it is necessary to provide amendments to the manual. If any amendments are provided for this manual, they are printed on colored paper and will be found at the rear of this manual.

NOTE: The content of any amendments may affect operation, maintenance, or calibration of the equipment.

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AUSTRON MODEL 2100 LORAN-C TIMING RECEIVER

1.0 GENERAL DESCRIPTION

1.1 SCOPE OF SECTION

This section introduces the AUSTRON Model 2100 Loran-C Timing Receiver. It is divided into three parts: (1) a description of the purpose of the equipment, (2) the physical and electrical specifications, and (3) an identification of the internal and external controls, indicators, and connectors.

1.2 PURPOSE OF EQUIPMENT

The AUSTRON Model 2100 Loran-C Timing Receiver automatically acquires and phase tracks Loran-C signals for time synchronization and frequency calibration and control. When monitoring Loran-C groundwave, sub-microsecond time synchronization to Universal Coordinated Time (UTC) can be made, and frequency measurements with an accuracy of several parts in 10^{12} are possible with one-day averaging.

1.3 SPECIFICATIONS

The AUSTRON Model 2100 Loran-C Timing Receiver is a microprocessor controlled Loran-C receiver. Programming for the Motorola M6802 microprocessor is contained in three EPROMS (UV eraseable-programmable-read-only-memory) on the MPU/MEMORY printed circuit board. In addition, there are 2048 bytes of random-access-memory (RAM), used for temporary data storage. All hardware is contained on seven plug-in printed circuit boards, an interconnect board, and a detachable front panel display board. The front panel is hinged at the bottom to permit access to the plug-in boards. Data entry and recall, and all receiver functions are handled through the numeric keypad, function switches and liquid crystal display on the front panel.

AC and DC power connectors, power switch, and various connectors for signals required by the receiver and signals generated by the receiver are located on the rear panel.

1.3.1 Physical Specifications

Height	3.5 inches (89 mm)
Width	17.0 inches (432 mm)
Depth	14.5 inches (369 mm)
Weight	15 pounds (6.75 kg) max.
Mounting	19 inch rack mountable with provisions for chassis slides.
Temperature	0° to 50°C operating -40 to +75°C storage

1.3.2 Electrical Specifications

Power	AC:	115/230 VAC, switch selectable, at 50 to 400Hz ±10% (35 watts).
	DC Standby:	+22 to +32 VDC, negative ground. Auto switch-over on AC failure. 1.5 amp at 22 VDC. 0.8 amp at 32 VDC.
Data Input		Numeric keypad and pushbutton function keys.
Data Output		Eight digit liquid crystal display (LCD). Light-emitting-diode (LED) status indicators.
RF Sensitivity		0.01 microvolt at receiver antenna input (50 ohms) at tracking point.
RF Bandwidth		40KHz, tracking. 4KHz, acquisition.

RF Gain	Automatic gain control with a dynamic range of 127dB.
1PPS Outputs Fixed:	Positive going pulse, approximately 0.4 seconds wide. Will drive 1 standard TTL load.
Slewable:	Positive going pulse, approximately 0.4 second wide. Will drive 1 TTL load. Slewable in steps of approximately 10 nanoseconds, minimum.
EXT REF INPUT (1, 5, 10MHz)	5VRMS (internally switch selectable) into 500 ohms, sine or square wave. Reference accuracy must be 5 parts in 10^6 or better for acquisition and track.
External 1PPS	TTL compatible input. Positive going edge must be the start of a second.
Phase Corrected 1MHz	Square wave output, will drive 1 standard TTL load.
Phase Corrected 10MHz	Square wave output, will drive 1 standard TTL load.
Scope Vertical	Buffered RF output to drive oscilloscope vertical input. Output impedance is less than 10 ohms, short circuit protected.

Scope Trigger	TTL compatible output. It will drive 1 standard TTL load.
Carrier Relay	Open collector output. 30 volts, maximum. 25mA sink, maximum.
Scan Strobe	Voltage output. ±5V, @ 5mA maximum. Indefinite short circuit duration to common.
Phase Record (1/10μsec)	Voltage output. 0-1V, 5mA maximum. Indefinite short circuit duration to common.
IEEE-488 (Option)	Meets IEEE-488-78 electrical and mechanical specifications.
Group Repetition Interval	GRI entered through front panel switches, from 29,184 microseconds to 102,910 microseconds, increments of 2 microseconds.
Track Servos	Second-order phase error loop.
Time Constants	Five selectable time constants.
Phase Servo Resolution	10 nanoseconds.
Time Interval Counter	Outputs to 0.01 microsecond. Accuracy = ±0.02 microsecond.

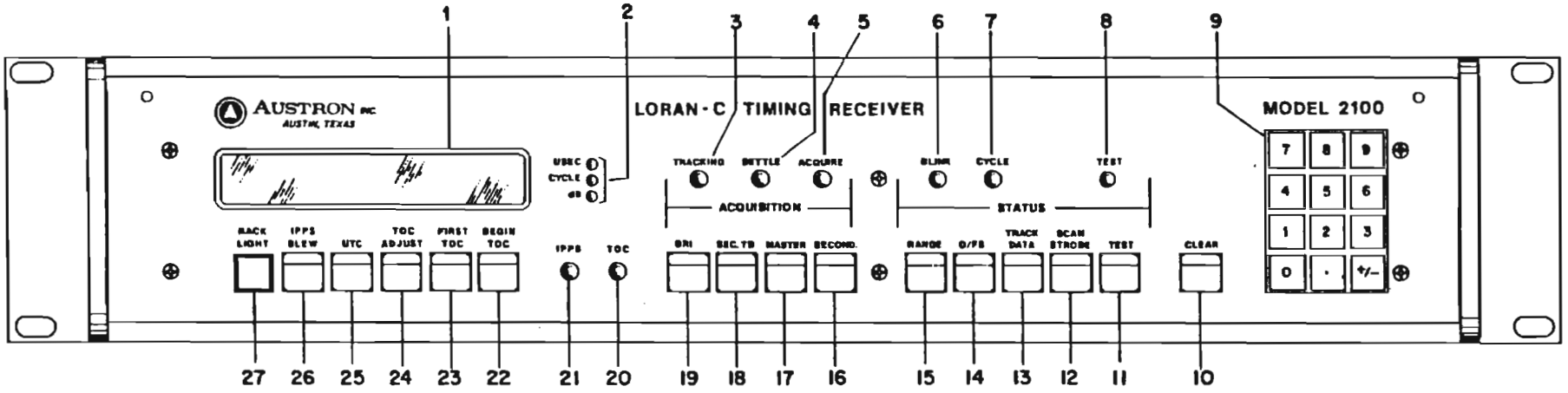
1.4 CONTROLS, INDICATORS, AND CONNECTORS

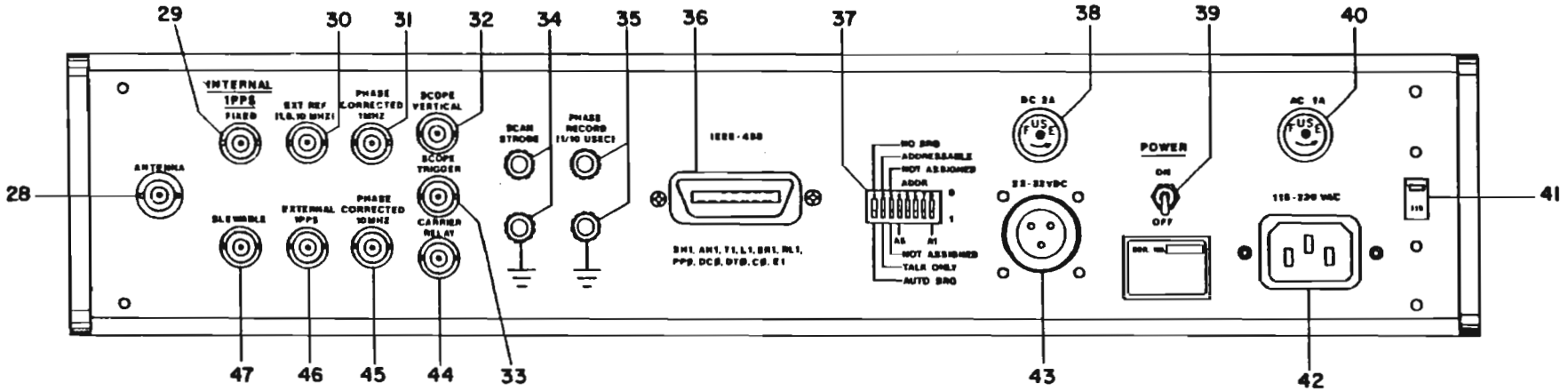
1.4.1 Figure 1-1 shows all controls, indicators, and connectors for the Model 2100. The following paragraphs contain brief descriptions of each input and output function. For a more detailed discussion of the operation of the Model 2100, please refer to section 3.0.

1.4.2 Front Panel

REF	DESCRIPTION	FUNCTION
1	Liquid Crystal Numeric Display	8 digit numeric display used for input/output of receiver control information, and output of calculated or measured data.
2	RED LED's	These LED's show the unit of the number being displayed.
3	TRACKING Red/Green LED	Green indicates normal tracking. Red indicates that the first order servo is locked. Alternating Red/Green indicates a problem with the Loran-C signal has occured which might affect the time or frequency measurement accuracy.
4	SETTLE Red LED	Receiver is settling to the normal tracking point after acquisition.
5	ACQUIRE Red LED	Receiver is attempting to acquire a Loran-C station.
6	BLINK Red LED	Indicates that the Loran station being tracked is "blinking."

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	9 5 81	





1-6

	2100		1-1
NEXT ASSY	USED ON	REF DES	FIG NO
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED		
DECIMALS	FRACTIONS	ANGLES
MATERIAL: N/A		
ENGR		8/11/81
CHECKED		8-5-81
DRAWN	LDP	8-5-81

AUSTRON INC.
AUSTIN, TEXAS

FRONT & REAR PANELS MODEL 2100

SIZE	CODE IDENT NO	
3	24672	12498864
SCALE 1:1		SHEET 1 OF 1

1.4.2 Front Panel (Continued)

REF	DESCRIPTION	FUNCTION
7	CYCLE Red LED	Indicates that the cycle number has changed by more than ±0.5 since the receiver entered the TRACKING mode.
8	TEST Red LED	Indicates that TEST subroutines are being run.
9	NUMERIC KEYBOARD Pushbuttons	Numeric keypad, including plus/minus and decimal point key, used for entry of receiver data.
10	CLEAR Pushbutton	Clears last numeric entry. Display changes back to previous output.
11	TEST Pushbutton	Function Key: controls operation of TEST routines.
12	SCAN STROBE Pushbutton	Function key: begins voltage output (rear panel, SCAN STROBE) of averaged Loran-C signal being tracked, to be used for third cycle verification.
13	TRACK DATA Pushbutton	Function key: controls output of various pieces of data and status information.

1.4.2 Front Panel (Continued)

REF	DESCRIPTION	FUNCTION
14	0/FS Pushbutton	Function key: Sets PHASE RECORD output (rear panel) to zero or one volt for calibration of external linear recorder. This key also causes the total receiver phase shift to be displayed.
15	RANGE Pushbutton	Function key: inputs and outputs the full scale range of the relative phase difference record output. Ranges allowed are 1 microsecond and 10 microseconds full scale.
16	SECOND Pushbutton	Function key: selects secondary Loran-C station for acquisition. Displays time-of-arrival difference of master and secondary.
17	MASTER Pushbutton	Function key: selects master Loran-C station for acquisition.
18	SEC TD Pushbutton	Function key: inputs and outputs approximate master-to-secondary time-of-arrival difference, used by the receiver to locate the secondary station to be tracked.

1.4.2 Front Panel (Continued)

REF	DESCRIPTION	FUNCTION
19	GRI Pushbutton	Function key: used to input and output the Group Repetition Interval (GRI) of the station to be acquired and tracked.
20	TOC Red/Green LED	Indicates current condition of the Time-of-Coincidence (TOC) function: a) OFF--TOC not active. b) Red and Green flashing -- TOC initiated, but first TOC has not yet occurred. c) Green on--Receiver has detected a Time-of-Coincidence at the predicted time-of-day. d) Red on--The Red LED is turned on one second before a TOC is to occur. If it remains on after one second, the receiver has detected a problem and the receiver may not be properly time synchronized.
21	1PPS Green LED	Indicates functioning of internal 1PPS.
22	BEGIN TOC Pushbutton	Function key: used to initiate the TOC sequence. Output is the next time-of-coincidence.

1.4.2 Front Panel (Continued)

REF	DESCRIPTION	FUNCTION
23	FIRST TOC Pushbutton	Function key: used to input the first TOC of the day (or any good TOC for that day). Output is the time entered on the last TOC time if TOC is active.
24	TOC ADJUST Pushbutton	Function key: input and display an adjustment (in microseconds) to be applied to the internal slewable 1PPS at the time of the first TOC. This adjustment will typically be the total-time-delay and will produce a one-pulse-per-second that is coincicent with Universal Coordinated Time. If no adjustment is to be applied, enter zero.
25	UTC Pushbutton	Function key: input and display the time-of-day. The internal clock is 24 hours and time is entered in Coordinated Universal Time (UTC).
26	1PPS SLEW Pushbutton	Function key: used to advance or retard the internal slewable 1PPS. Output is the measured time difference between the internal non-slewable 1PPS and the slewable 1PPS.

1.4.2 Front Panel (Continued)

REF	DESCRIPTION	FUNCTION
27	BACK LIGHT Pushbutton	Function key: turns on the LCD backlight for approximately 2 minutes from the last time the switch was pushed.

1.4.3 Rear Panel

REF	DESCRIPTION	FUNCTION
28	ANTENNA Isolated BNC Connector	Antenna input connector. Input impedance is 50 ohms.
29	1PPS FIXED BNC Connector	TTL compatible 1PPS output, approximately 0.4 second wide, phase corrected to the received Loran-C signal. If a TOC sync has been done, the positive going edge of this pulse will be delayed from UTC by the total timing delay.
30	EXTERNAL 1MHz BNC Connector	Input connector for external receiver reference. The reference can be 1, 5, or 10MHz, 0.5 to 5VRMS, sine or square wave.
31	PHASE CORRECTED 1MHz BNC Connector	Phase shifted 1MHz output. This square wave output is corrected to the received Loran-C signal and will drive one standard TTL load.

1.4.3 Real Panel (Continued)

REF	DESCRIPTION	FUNCTION
32	SCOPE VERTICAL BNC Connector	Oscilloscope vertical output connector. This is the amplified, filtered, and buffered antenna input signal which is being tracked by the receiver. An abrupt vertical displacement of the RF indicates the current tracking point.
33	SCOPE TRIGGER BNC Connector	Oscilloscope trigger output connector. This is a TTL compatible positive pulse used to trigger the sweep of an external oscilloscope.
34	SCAN STROBE Banana Plugs	Scan Strobe output connector. When requested, the receiver outputs a DC voltage which slowly oscillates about 0 volts as the tracking strobe scans through the Loran-C pulse. This output will drive a linear chart recorder (must be able to take ±5 volts) to produce a highly filtered representation of the Loran-C pulse, for cycle verification. The output will momentarily return to zero volt when the current tracking point and the moving strobe coincide. During this scan, tracking is suspended, but the second order correction (external reference frequency offset) is still applied.

1.4.3 Real Panel (Continued)

REF	DESCRIPTION	FUNCTION
35	PHASE RECORD 1/10µsec Banana Plugs	Voltage representation of accumulated phase shift. This output ranges from 0-1 volt and represents an accumulation of 1 or 10µsec at full scale.
36	IEEE-488 Connector	General Purpose Interface Bus (GPIB) (IEEE-488-1978) provides remote control capability. See section 4.0.
37	IEEE-488 Address Switches	Used to select the bus address for the Model 2100. See section 4.0.
38	FUSE DC 2A	Fuses internal unregulated DC when operating from external AC or DC source.
39	POWER Switch	AC/DC power switch.
40	FUSE AC 1A	Fuses external AC input line.
41	115-230 VAC Selector Switch	AC voltage selection switch.
42	115-230 VAC Connector	Input connector for 115/230 VAC external power.
43	22-32 VDC DC Standby Connector	Input connector for an external +22 to +32 VDC standby power source.

1.4.3 Rear Panel (Continued)

REF	DESCRIPTION	FUNCTION
44	CARRIER RELAY BNC Connector	Carrier relay output connector. This is an open collector output which is low (transistor on) when the tracking servos are locked, and high (transistor off) when the servos are active.
45	PHASE CORRECTED 10MHz BNC Connector	Phase shifted 10MHz output. This square wave output is corrected to the received Loran-C signal and will drive one standard TTL load.
46	EXTERNAL 1PPS BNC Connector	1PPS sync input connector. Accepts a TTL level 1PPS to synchronize the internal 1PPS and to do the first TOC synchronization.
47	1PPS SLEWABLE BNC Connector	TTL compatible 1PPS output, approximately 0.4 second wide, phase corrected to the received Loran-C signal. This 1PPS output can be slewed using the 1PPS SLEW function switch.

2.0 INSTALLATION

2.1 SCOPE OF SECTION

2.1.1 This section describes the steps required to prepare the Model 2100 Loran-C Timing Receiver for operation, or reshipment to another location. Included are steps for unpacking, inspection, and a list of fundamental electronic requirements and accessories.

2.2 Unpacking and Inspection

2.2.1 Unpacking -- Carefully remove the Model 2100 from its shipping container. Verify that the serial number on the receiver matches the number on the packing list. If it does not match, contact AUSTRON, INC. immediately. Locate the following accessories:

a) Mating DC Standby input connector (Customer must supply standby power cable).
b) Spare fuses, 1 amp, 5 each.
c) Spare fuses, 2 amp, 5 each.
d) Three-wire 115 VAC power cord.
e) Technical manual.

In addition, locate any optional equipment that should come with your unit, such as spare boards, extra manuals, spare integrated circuits, etc. Report any discrepancies to AUSTRON, INC.

2.2.2 Initial Inspection -- Immediately report any equipment damage to the carrier making delivery, and to AUSTRON, INC. Inspect internal components by removing top cover (secured by 4, ¼ turn fasteners). Before connecting the power cords, examine the interior for loose or broken parts. Remove the packing material between the front

panel and the top of the printed circuit boards (save for use when reshipping). Unscrew the two thumbscrews securing the front panel and lower the panel. Remove and inspect each of the small boards on the right side. Be careful to replace each board in its original slot. Carefully disconnect the large ribbon cable from the back of the front panel printed circuit board. Remove and examine each of the large printed circuit boards for any apparent damage. All components, except the EPROMS, U41, U42, and U43 on the MPU/MEMORY PCB, are soldered in place. Any loose components should be reported immediately. Replace the large boards and reconnect the cable. Replace the top cover and close the front panel.

2.3 Installation

2.3.1 Reference Figure 2-1. The Model 2100 receiver requires four things for normal operation. First, a suitable antenna (AUSTRON Model 2021L or Model 2026W) must be connected to the receiver antenna input by a 50 ohm coaxial cable. Refer to section 3.3 for a discussion of antenna selection, location, and orientation. Second, a frequency source of 1, 5, or 10MHz must be connected to the reference input. This source must have an accuracy of 5 parts in 10^8 or better. Third, an AC voltage source of 115/230 VAC ±10% at 50Hz to 400Hz or a DC source of 22 to 32V must be provided. The use of an external DC standby power supply is recommended when uninterrupted operation is desired. Fourth, an external time-of-day reference, accurate to within 10 milliseconds of Coordinated Universal Time (UTC), is necessary to achieve Time-of-Coincidence (TOC) synchronization of the Model 2100 with the selected Loran-C station. The National Bureau of Standards radio station WWVB or an equivalent reference may be used for a time-of-day setting and for coarse "on-time" 1PPS setting. See section 3.6 for a detailed discussion of time synchronization.

2.3.2 Additional receiver setup involves the MPU/MEMORY printed circuit board (large digital pcb in the bottom slot, 10398079). If the revision level of the printed circuit board is C or later, there are two options which can easily be selected on this board. To determine the revision level, turn power off, lower the front panel and disconnect

the two ribbon cables, and remove the pcb from the chassis. On the foil side, in the upper right-hand corner, there is a number, 00398078. The revision level is shown inside a box to the left of this number.

2.3.2.1 The first option involves the input impedance of the EXT REF (1, 5, 10MHz) buffer. As shipped from the factory, the impedance is approximately 500 ohms. It can be lowered to 50 ohms by shorting across the solder gap, W1, on the foil side of the board. This should properly terminate any frequency source which is intended to drive a 50 ohm load.

2.3.2.2 The second option determines the output characteristics of the CARRIER RELAY. The model 2100 is shipped with the CARRIER RELAY output set up as an open collector driver (W2 and W3 open). If the receiver is to be used with an AUSTRON Model 6016, Model 6014, or Model 6014B, or with any other equipment requiring a 0 volt to +12 volt output, short across solder gap, W2, on the foil side of the board (W3 open). This connects the collector of Q3 to +12 volts through a 4.7K ohm resistor. When the receiver is tracking normally, this output will be approximately +12 volts. When the servos are locked, indicating loss of signal, the CARRIER RELAY will be at 0 volts (may be as high as 0.5 volt). If W3 is shorted and W2 open, the CARRIER RELAY output will behave as described above, except that the maximum output level is 5 volts, making it TTL compatible.

2.3.2.3 If the revision level of the MPU/MEMORY circuit board is less than Revision C, these options can still be utilized. However, it will involve installing additional resistors on the foil side of the board. A 56 ohm, ¼W 10% resistor installed from the input of the EXT REF buffer to ground will reduce the input impedance to 50 ohms. The input of the buffer is the buffer side of capacitor C1. To implement the CARRIER RELAY option, determine what voltage is required (see section 2.3.2.2). If a 5 volt output is required, connect a 1K, ¼W 10% resistor from the collector of Q3 to the closest source of +5 volts (probably U11 pin 16). Insulate the leads to prevent shorting. If a +12 volt output is needed, connect a 4.7K, ¼W 10% resistor from the collector of Q3 to U10 pin 9.

2.3.3 The Model 2100 Receiver is shipped with rack ears for mounting in a standard 19 inch rack. Provisions have also been made for chassis slides. (CHASSIS TRAK C-230-S-116 through -124 or equivalent). If the receiver is not to be rack mounted, it should be placed on a stable surface close to the frequency source.

2.3.4 Before connecting power to the receiver, make sure the power switch on the rear panel is in the OFF position. Also, set the AC voltage switch to the voltage to be used (this switch is set in the 115VAC position at the factory). Connect the AC and/or DC power cables to the receiver. If operation of the unit in the event of line power failure is desired an auxiliary DC power source capable of supplying from 22-32 VDC at 1.5 amps, must be connected to the rear panel DC standby input. The mating connector for the DC standby input is supplied with the accessory kit and should be wired as shown below with 20 AWG or larger wire.

Pin A	Battery positive
Pin B	Battery Negative
Pin C	Not Connected

2.3.5 Before turning power on, connect the antenna, reference frequency, and external 1Hz signals to the receiver. If a frequency source other than 1MHz is used, open the front panel and set the toggle switch, located on the top edge of the MPU/MEMORY PCB, to the appropriate frequency (i.e., 1, 5 or 10MHz). Close the front panel. Refer to section 3.0 for operating instructions.

NOTE: When viewed from the front of the Model 2100 receiver (front panel lowered) the left most position of the reference frequency select switch corresponds to a 1MHz input, the center corresponds to a 10MHz input, and the right most position corresponds to a 5MHz input. If the switch position and the reference frequency do not agree, the receiver may be able to acquire and track a Loran-C signal (with greater difficulty), but the time-of-day clock will gain or lose time.

2.4 Preparation for Reshipment

2.4.1 Disconnect all external cables. Check to see that all mounted components are in place and securely tightened. All printed circuit boards and internal cables should be tightly inserted in their respective connectors. Packing material should be inserted between the top of the printed circuit boards and the back of the front panel to prevent them from becoming disconnected in shipment.

2.4.2 For shipping, enclose the Model 2100 in a suitable water and vapor proof plastic bag. Projections, sharp edges, and other features which might tear or puncture the plastic, should be padded. Chassis slides should be removed and packed separately. Heat seal or tape the plastic bag to ensure a moisture-proof enclosure. When sealing the bag, keep the trapped air volume to a minimum.

2.4.3 The shipping container should be a rigid box of sufficient strength and size to protect the equipment from damage. The original shipping container and packing material may be reused if still in good condition.

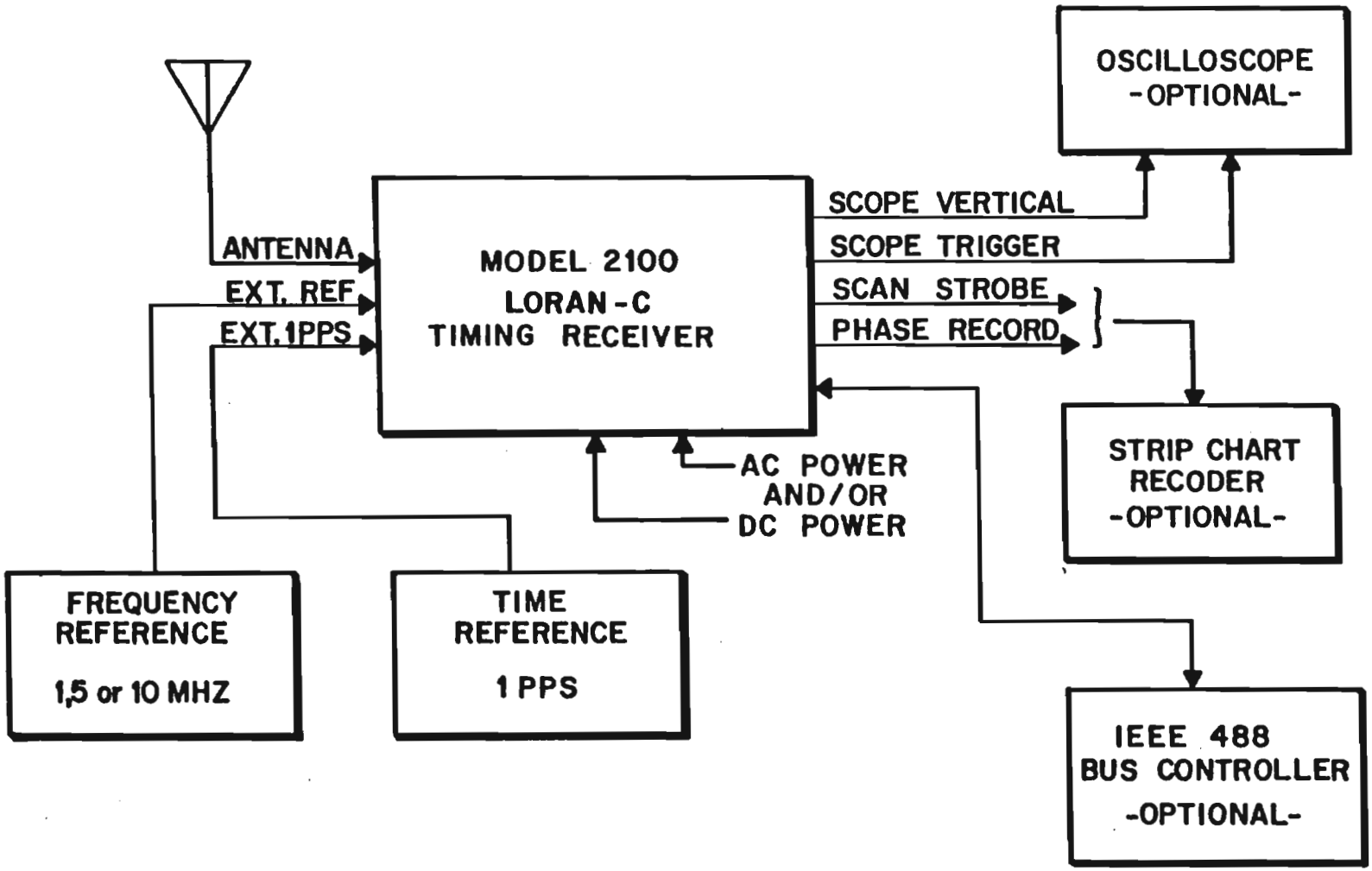


FIGURE 2-1

TYPICAL OPERATIONAL INTERCONNECTIONS

3.0 OPERATING INSTRUCTIONS

3.1 SCOPE OF SECTION

3.1.1 This section describes the operation of the AUSTRON Model 2100 Loran-C Timing Receiver. A discussion of other uses and procedures is also included. It will be assumed that the receiver has been set up as described in section 2.0. A thorough understanding of the Loran-C system is not necessary to acquire and track a station using the Model 2100. However, it is recommended that the user become familiar with the material in the appendix before continuing with this section.

3.2 GENERAL RECEIVER OPERATION

3.2.1 Turn the receiver power on. After about ½ second the LED indicators will turn off and the status of the random access memory (RAM) and the program memory (EPROM) will be displayed. The RAM status should be indicated by E1002048, which means the RAM is working. The EPROM status is shown next and should be E-20. For any other output, refer to the maintenance section, 6.0. After the memory status is displayed, the internal time-of-day clock is displayed (initialized to zero). If no errors were detected in the receiver memory, the Model 2100 is now ready for operation.

NOTE: It is possible that most or all of the receiver functions will operate properly if a memory problem has been detected. However, the bad memory should be replaced as soon as possible.

3.2.2 Normal operation of the Model 2100 will not require the use of an oscilloscope. However, it may be helpful to use one while becoming familiar with the receiver. Oscilloscope VERTICAL and TRIGGER outputs are located on the rear panel. The vertical output is the amplified Loran-C signal and all signals within the 40KHz bandwidth of

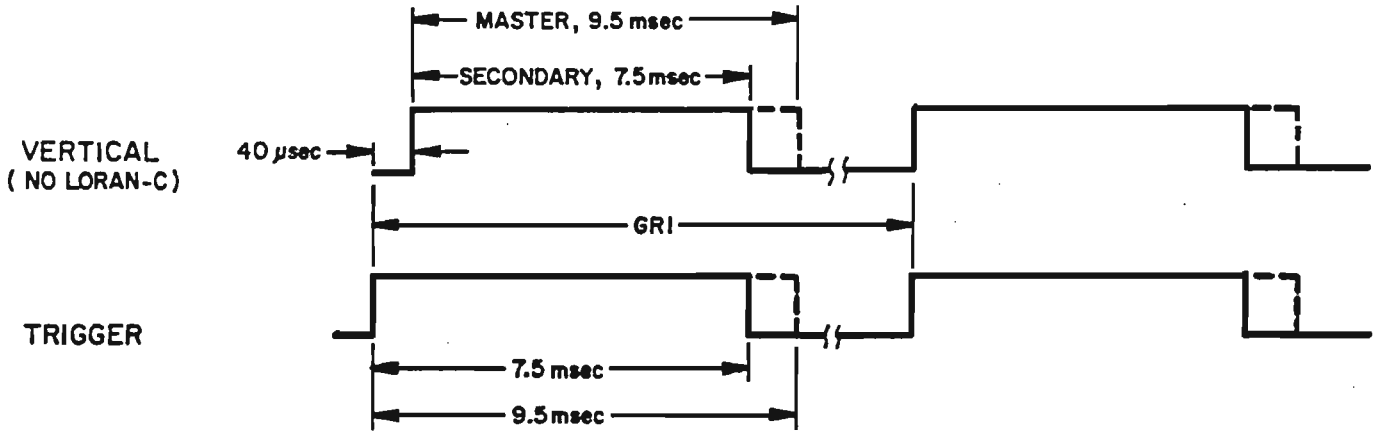
the main tracking filter (centered at 100KHz). Connect the VERTICAL and TRIGGER outputs to the corresponding oscilloscope inputs. Adjust the vertical and timebase controls to give a trace as shown in figure 3-1a. With no RF there will only be a step, approximately 1 volt peak and 7.5 or 9.5 msec wide (secondary or master). The start of this step is delayed 40 usec after the trigger. With RF, the oscilloscope trace will look like figure 3-1b, when the receiver is in the TRACKING mode. Note that the Loran-C signal and the pulse are added together; causing the vertical displacement of the Loran-C at the beginning of the step. This identifies the normal tracking point and will be at the start of the fourth cycle of the first Loran-C pulse.

3.2.3 Data Input/Output -- The Model 2100 Loran-C Timing Receiver is simple to use and requires little operator attention. However, some information must be input by the operator and the measurements and calculations must be displayed. Data is entered into the numeric display through the numeric keypad. If the data is valid, it is transferred to memory by pushing one of the white "function" buttons. To display information associated with a particular "function" button, push that button.

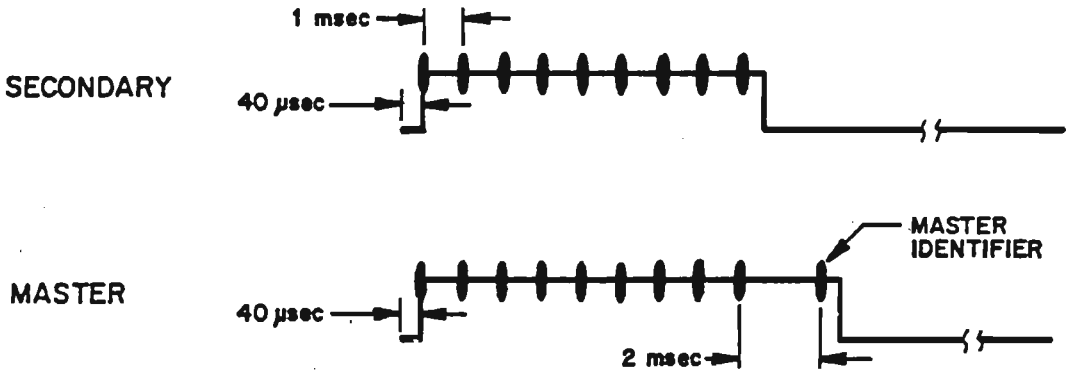
EXAMPLE: To enter a GRI of 99,600 microseconds, push keys 9,9,6,0,0. The display should show these 5 digits. Push the "function" button, GRI. Because 99,600 is in the range of valid GRIs, the receiver accepts the GRI and turns on the USEC LED. If an attempt is made to enter data that is out of range, the display will read, --HELP--, and the front panel controls will be disabled until the CLEAR button is pushed.

3.2.4 Function Key Description -- The function keys are used to input and output information and to control the operation of the receiver. The following paragraphs describe each of these buttons, including their purpose, limits, and receiver response.

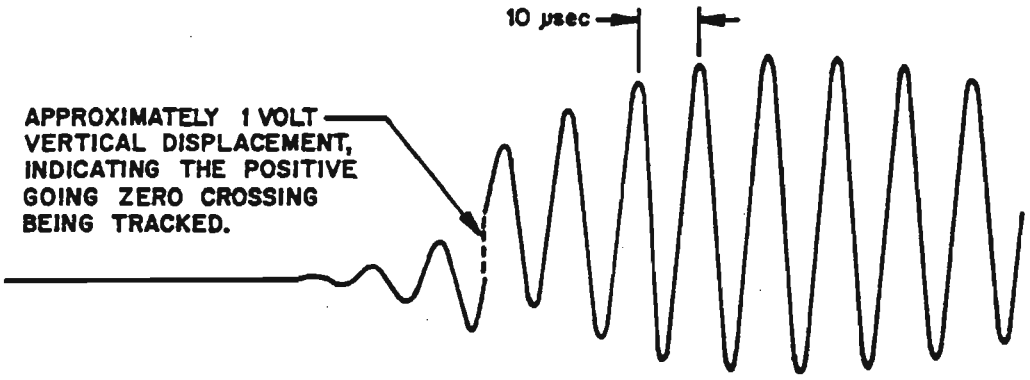
A) BACKLIGHT -- The BACKLIGHT key turns on the liquid crystal display backlight to improve readability in low ambient light conditions. The backlight stays on for 128 seconds from the last time the key was pushed. No input is allowed and no information is displayed.



a. *OSCILLOSCOPE OUTPUTS*



b. *EXAMPLE OF RECEIVER LORAN-C SIGNAL*



c. *LORAN-C PULSE*

Figure 3-1. Model 2100/F Oscilloscope Output

B) 1PPS SLEW -- This key is used to advance or retard the "slewable" 1PPS and to synchronize the "slewable" and "fixed" pulses to the external 1PPS. The amount of slew should be limited to no more than ±499,999.99 μsec. The output of this key is the measured time interval between the "slewable" 1PPS and the "fixed" 1PPS. The output is negative when the "fixed" 1PPS occurs after the "slewable" 1PPS, and positive when the "fixed" 1PPS occurs before the "slewable" 1PPS. When this output is selected there will be a three to four second delay before the time interval is displayed.

C) UTC -- The time of day, in Universal Coordinated Time, is input and output by this key. The time is in 24 hour format. An entered time greater than or equal to 24:00:00 will cause the error display, --HELP--.

D) TOC ADJUST -- TOC ADJUST is the amount of slew to be applied to the "slewable" 1PPS after the first TOC synchronization. It should be limited to no more than ±499,999.99 μsec. The output is equal to the last input.

E) FIRST TOC -- FIRST TOC is the first TOC of the day as determined from the USNO TOC tables and entered by the operator. This may also be any good TOC for the date the synchronization is done. If 24 hour format is not used, the error display, --HELP--, will result. The output is equal to the last input, until a TOC time occurs. At each time-of-coincidence, the current TOC time is transferred to FIRST TOC when the next TOC time is calculated.

F) BEGIN TOC -- The only input allowed for this key is 1 or 0. An input of 1 starts the synchronization (TOC LED alternating between red and green) and an input of 0 stops it. No other input is allowed. The output is the next time-of-coincidence.

G) GRI -- This key is used to input and display the Group Repetition Interval (GRI). The GRI can range from 29,184-102,910 μsec, in steps of 2 μsec. An out-of-range GRI will cause the error display, --HELP--. When a GRI is entered, TRACKING and TOC are halted.

H) SEC.TD. -- SEC.TD. is used to input and display the approximate hyperbolic time difference used for acquisition of a specific secondary. This number must always be positive and must not exceed the GRI.

I) MASTER -- This key starts or stops master acquisition and track. An input of 1 starts acquisition. An input of 0 stops acquisition or track. All other inputs cause the error display --HELP--. If the master station is not being tracked, the output will be "--------". If active, the output is 0.

J) SECOND -- This key starts secondary acquisition if 1 is entered, and stops secondary acquisition if 0 is entered. All other inputs cause the error display, --HELP--. If a secondary is not being tracked, the output is "--------". If this function is active, the display will be the measured approximate hyperbolic time difference, which can be used to determine

which secondary is being tracked. This output will be within ±5 msec of the number entered through the SEC.TD. function, if SEC.TD. is not zero.

K) RANGE -- The full scale range of the accumulated phase shift can be set to either 1 or 10 μsec. No other ranges are allowed. The accumulated phase shift is available on the rear panel as a voltage ranging from 0 to 1 volt.

L) 0/FS -- 0/FS (read, zero/full scale) is used to calibrate the linear chart recorder used to record the accumulated phase shift. An input of zero causes an output to the recorder of zero volt; an input of one causes an output of one volt. After calibrating the recorder, the 0/FS key must be pushed once more to output the accumulated phase shift to the front panel and to the connector on the rear panel. If this is not done, the last calibration voltage will remain.

M) TRACK DATA -- TRACK DATA is a collection of ten items, including receiver control instructions and data. Functions are activated or data is recalled by pushing TRACK DATA, then the number (0-9) of the response desired.

TRACK DATA	DESCRIPTION
1	This causes the receiver to lock out the front panel to prevent unauthorized or accidental loss of track or TOC.

0

The keyin, TRACK DATA 0, enables the front panel if it had been locked by TRACK DATA 1. If the panel is not locked out, the error display, --HELP--, results.

2

This keyin displays the noise number while the receiver is in the TRACKING mode. The relationship between the noise number and the signal-to-noise-ratio is approximately as follows:

SNR (dB)	Noise Number
+9	4
+6	7
+3	14
0	28
-3	56
-6	112
-9	224
-12	448
-15	896
-18	1792
-21	3584

No input is allowed for TRACK DATA 2.

3

TRACK DATA 3 displays the receiver gain. This output can range from 0 to 127 dB. High gain indicates low signal strength. No input is allowed.

4

This keyin displays the calculated frequency offset. It ranges from ±1 part in 10^6 to ±1 part in 10^{13}. No input is allowed.

5

TRACK DATA 5 displays the cycle number while the receiver is in the TRACKING mode, and "--------" while not in the TRACKING mode.
This keyin is also used to move the tracking point forward or backward up to 6 cycles, to correct for being on the wrong cycle. To move the tracking point ±X cycles, enter ±X TRACK DATA 5. Within 6 seconds the tracking point will have been moved the desired amount. Then, depending on the noise and the receiver time constant, there will be a delay before the tracking point can be moved again. During this delay, new nominal gain and cycle numbers are calculated.

6

TRACK DATA 6 is used to input and display the receiver time constant. When power is applied, the time constant is set to two. Another time constant can be entered by keying in, X TRACK DATA 6, where X is the new time constant (0-4). The response time in GRIs is:

TIME CONSTANT	GRIs
0	3200
1	1600
2	800
3	400
4	200

No other inputs are allowed.

7 TRACK DATA 7 is used to display accumulated receiver phase shift. The only entry allowed is zero, to reset the phase shift. This only sets this output to zero and has no effect on the tracking point or on the linear output on the rear panel.

8 TRACK DATA 8 displays the receiver status (see section 3.5). The only input allowed, 0 TRACK DATA 8, clears the errors.

9 This keyin displays the time difference between the internal "fixed" 1PPS and the external 1PPS. No input is allowed.

N) SCAN STROBE -- SCAN STROBE starts or stops the receiver scan of the Loran-C pulse, used for manual verification of the third cycle tracking point. An input of from 1 to 6 followed by pushing SCAN STROBE, starts the receiver scan. The length of the scan and the amount of averaging increases as the number of input increases. To stop the scan, enter 0 SCAN STROBE. See section 3.7 for a complete explanation of cycle determination using the Loran-C scan.

O) TEST — This key controls the test subroutines. See section 6.0 for details.

P) CLEAR — This key is used to clear a previous numeric entry. The display changes back to the last output.

3.3 ANTENNAS, NOISE, AND TIME CONSTANTS

3.3.1 For proper operation of the Model 2100 Loran-C Timing Receiver, a suitable antenna, properly installed, must be connected to the antenna input on the rear panel. There are two antennas recommended for use with the Model 2100. They are the AUSTRON Model 2021L Loop Antenna and the AUSTRON Model 2026W Whip Antenna. The preferred antenna is the 2026W Whip, because it is nondirectional, allowing reception of all signals at the receiver location, and it has less signal loss than the 2021L Loop. Other antennas can be used with the Model 2100, but are not recommended. Cycle selection problems may be introduced, because of the response of these other antennas.

3.3.2 For time synchronization, it is important to know which station is being tracked (section 3.4). If a master station is selected, no identification problem exists, and either antenna may be used. If, however, a secondary station is desired, the Model 2100 must be able to simultaneously receive the master and the secondaries. If a loop antenna is used, it may cancel the master signal, because of its directionality, making it impossible to acquire the desired secondary.

3.3.3 If a whip antenna is used, it is easy to change stations being tracked. The operator enters the information for the new station and restarts acquisition. If a loop is used, it may also be necessary to rotate the loop toward the new station to maximize the signal strength.

3.3.4 Despite its limitations, the loop antenna may be the best antenna for some locations. Conditions which would favor use of a loop antenna are:

1) Strong, nearby transmitter, operating in or near the bandwidth of Loran-C (roughly 90-110KHz). In this case, the loop would be positioned to null the interferring signal, while preserving the Loran-C signal,and

2) suitable receiver and Loran-C station geometry. That is, all stations required are in roughly the same place as the loop, so that the loop does not completely null the master when it is pointed toward the secondary of interest.

3.3.5 When either antenna is installed, it should be located away from other antennas and large metal objects. If possible, it should be high enough to clear objects in the near vicinity and the base should be connected to a good earth ground. A loop should be rotated so the arrow on the antenna base points towards the station to be tracked. After the TRACKING mode is entered, rotate the loop to obtain maximum signal, or, if necessary, to obtain the best compromise between signal strength and noise.

3.3.6 There are several sources of noise which may influence Loran-C reception. These include atmospheric noise, receiver noise, carrier wave (CW) interference, and cross rate interference. The first two sources, atmospheric and receiver noise, must usually be tolerated, since the operator has little or no control over them. Unless the signal is very weak, these noise sources will usually cause few problems.

3.3.6.1 Crossrate interference is noise caused by Loran-C signals that have different Group Repetition Intervals (GRI) from the station being tracked. Because of the difference in intervals, there are times when the tracked and interfering Loran-C signals overlap, producing variations in the sampled signal. In areas where stations with different GRIs can be received, the GRIs have been selected to minimize the frequency and duration of overlap. Cross rate interference is usually not a major problem.

3.3.6.2 Of the noise sources mentioned, carrier wave interference is probably the most significant. The 40KHz bandwidth filter in the receiver will effectively reduce frequencies below 80KHz and above 120KHz. However, frequencies outside this range may still cause acquisition problems if the signal is strong enough. Frequencies outside the bandwidth of Loran-C (90-110KHz) can be effectively reduced by using a loop antenna or by installing notch filters. For frequencies within this range, it is probably best to use just a loop antenna. Use of notch filters within the Loran-C frequency range should be avoided because they will cause distortion of the Loran-C envelope, affecting acquisition.

CAUTION: Notch filters will introduce additional delay which must be accounted for if time synchronization to better than 10 μsec is desired.

3.3.7 Because of noise, the tracking point of the Loran-C signal, and therefore, the synchronized 1PPS, may vary by ±50 nsec. To reduce the jitter, a longer time constant can be selected which will reduce the receiver response to short term changes.

3.3.7.1 When power is turned on, the time constant is set to a nominal value of 2. This will provide good receiver response when the accuracy of the external reference is better than one part in 10^9 and the signal-to-noise ratio is better than -10 dB. The reference accuracy is important, because the receiver must be able to keep up with the reference. If the time constant is too long the receiver may not be able to maintain lock. Longer time constants of 1 or 0 can be used when the accuracy of the reference is better than one part in 10^{10}. The shorter time constants, 3 and 4, should be used if the reference accuracy is worse than about one part in 10^8. This is particularly true during acquisition. After the receiver has been in the TRACKING mode for about 30 minutes, a longer time constant can be used, because the receiver will have "learned" the frequency offset and should then be able to maintain lock.

3.3.7.2 The time constant can be examined by pushing TRACK DATA, then 6. To change the time constant, enter the new time constant,

then push TRACK DATA, 6.

3.4 ACQUISITION AND TRACK

3.4.1 STATION SELECTION -- For accurate time synchronization with Loran-C, it is necessary to know which station is being tracked so that all delays, transmission, propagation and antenna/receiver, can be taken into account. Using the Loran-C coverage chart in the appendix, select the closest transmitter and enter its Group Repetition Interval (GRI) into the receiver. If a master was selected, no other information is necessary and acquisition can proceed as described in section 3.4.2.

3.4.1.1 If a secondary was chosen, a second number must be entered into the Model 2100 to specify which secondary is to be acquired. This number is the approximate time difference between the arrival of the master signal at the receiver site and the arrival of the secondary signal to be tracked. In the Loran-C navigation community, this number is called a hyperbolic time difference and, if measured accurately, it is one half of the information needed for a Loran-C navigation fix.

3.4.1.2 For the Model 2100 Loran-C Timing Receiver, this time difference needs to be known to within ±5 msec. In almost all locations, it can be approximated by entering the Total Emission Delay (TED) given in Table A-1 in the appendix. Locate the GRI and name of the secondary to be tracked in the table. Enter the TED to the nearest 1000 μsec and push SEC.TD.

EXAMPLE:		
	Receiver site	= Dallas, Texas
	GRI	= 79800 USEC
	Secondary to be tracked	= Grangeville, LA
	Total Emission Delay	= 12809.54 USEC
	Enter 1,3,0,0,0, SEC.TD.	

3.4.1.3 For this station selection process to work, the Model 2100 receiver must be able to locate the master, since it uses the time

of arrival difference and the approximate time difference (SEC.TD) to differentiate between other secondaries on the same GRI. If the master cannot be found, however, it may still be possible to know which secondary is being tracked. Enter 0, SEC.TD. This will cause the Model 2100 to acquire and track the best secondary it can find. One of the following methods can be used to identify the secondary being tracked.

a) If a loop antenna is used, it may be possible to orient it so that the secondary of interest is much stronger than any other secondary in the chain. This will increase the probability that that secondary will be selected.

b) After the receiver has settled to the TRACKING mode, do a time of coincidence synchronization. Using an external 1 hertz signal which is synchronized to Universal Coordinated Time to within 2 msec, measure the time interval from the "on time" 1PPS to the TOC-synchronized 1PPS from the Model 2100. Because no two secondaries are transmitted at the same time, the time interval from a UTC second to a TOC-synchronized second will be unique for each secondary, and will be equal to the Total Emission Delay shown in table A-1 at the secondary transmitter (less antenna, receiver and cycle delays). As the receiver is moved away from the transmitter, the time interval increases by an amount equal to the RF propagation time from the transmitter to the receiver. The difference between the two time intervals for adjacent secondaries will vary as the receiver site is changed. However, they should never be closer than about 9 msec, making it possible to identify the secondary being tracked.

3.4.2 ACQUISITION -- After the GRI and SEC.TD. have been entered, the receiver is ready for acquisition. To start acquisition enter 1, then push MASTER for master acquisition, or SECOND for secondary acquisition. The numeric display should be "0" and the ACQUIRE LED should be on.

3.4.2.1 During the acquisition period the receiver locates all of the Loran-C signals present at the receiver site, which have the Group Repetition Interval entered by the operator. This process typically takes 25-45 seconds, depending on the GRI. After the stations are located, one is selected, based on the operator keyins, and the SETTLE mode is entered.

3.4.2.2 Acquisition is a discrete process requiring 25-45 seconds, if the desired station is found on the first try. If a selection cannot be made after the first try, acquisition is repeated (another 25-45 second period). This process of "search and select" will continue until the desired Loran-C station is found or until acquisition is stopped by the operator.

3.4.2.3 The SETTLE mode should be reached within 15-20 minutes, even if the signal-to-noise ratio is low. If the SETTLE mode has not been reached after 30 minutes, the following procedure should be used to attempt to correct the problem:

a) GRI: Recall the Group Repetition Interval by pushing the GRI function key. For best results, the closest station should be tracked. If the GRI is not correct, enter the correct GRI. There will be a short delay, then acquisition is stopped.

b) MASTER: If the master station is be acquired, continue with d, below.

c) SECOND: If a secondary station is to be tracked, recall the approximate time-of-arrival difference by pushing the SEC.TD. function key. If necessary, enter the correct SEC.TD. for the secondary to be acquired (see sections 3.4.1.1, 3.4.1.2, and 3.4.1.3). If SEC.TD is zero, continue with d, below. If a particular secondary is to be acquired (SEC.TD. not zero), it may be necessary to use a SEC.TD. that is slightly different from that determined in section 3.4.1.2. However, before trying a different SEC.TD., complete d, below and try acquisition at least once more. If this has been done, two alternate approximations for SEC.TD. should be tried. Increase the approximation determined in section 3.4.1.2 by 2500 usec and attempt acquisition. If this does not help, decrease the initial approximation by 2500 usec and try acquisition. At this point, if SETTLE has not been reached, there are several possible reasons for the lack of success. First, the desired station may be too far away or the signal-to-noise ratio may be less than about -10 dB. It may be possible to improve the signal-to-noise ratio by moving the antenna away from noise sources such as power lines and transmitters. Second, it may not be possible for the receiver to locate the master. To remedy this, set SEC.TD. to zero and use one of the methods discussed in section 3.4.1.3 to identify the secondary being tracked. Third, there may be a hardware failure in the receiver.

d) Hardware: Make sure the antenna is located away from noise sources and the coupler housing is connected to a good ground. Check the antenna connection on the rear panel of the receiver. Finally, be sure that a suitable reference is connected to the EXT REF input and that the toggle switch on the MPU/MEMORY circuit board is set to the same frequency as the external reference. Retry acquisition.

3.4.3 SETTLE -- After selecting a Loran-C station, the receiver enters the SETTLE mode. The ACQUIRE LED goes off and the SETTLE LED comes on. In this mode the receiver locates the end of the third cycle of the Loran-C pulse (normal tracking point) and settles to the zero crossing of the 100KHz carrier. The nominal values for receiver gain and Loran-C cycle number, used to determine error conditions in the TRACKING mode, are established during this period. Averages for relative noise and BLINK, and a preliminary value of frequency offset are calculated.

3.4.3.1 The length of time the receiver remains in the SETTLE mode is determined by the receiver time constant and the signal-to-noise ratio, with the signal-to-noise ratio causing the greatest variation in the SETTLE time. If the SNR is better than +10 dB, the receiver will usually settle to the TRACKING mode in less than 5 minutes. For a SNR of -10 dB, the settle time may be as long as 30 minutes. If the TRACKING mode has not been reached after about 60 minutes, acquisition should be restarted.

3.4.4 TRACKING -- When the Model 2100 leaves the SETTLE mode and enters the TRACKING mode, the SETTLE LED goes out and the green TRACKING LED comes on. In this mode, all outputs, hardware and calculated, are available and the Loran-C signal is continuously monitored for error conditions such as BLINK, CYCLE error, and loss of signal. A time-of-coincidence synchronization can now be done and the receivers "slewable" 1PPS can be synchronized to Universal Coordinated Time.

3.5 TRACK AND STATUS INDICATORS

3.5.1 When the Model 2100 enters the TRACKING mode, the TRACKING LED turns green. If a possible problem with the Loran-C signal or the receiver is detected, the TRACKING LED will either alternate between red and green, or will be on continuously. The error conditions checked for are discussed in section 3.5.3.

3.5.2 The occurance of an error condition is indicated in two ways. LED indicators on the front panel show the current status of the receiver. When a problem occurs, the appropriate LED is turned on as an immediate indication. For three errors, including BLINK, CYCLE, and loss of signal, the indicators are turned on when the error begins and off when it ends. The TRACKING LED begins alternating when the error begins and continues alternating after the error condition passes.

3.5.2.1 The status of TOC is indicated by the TOC LED. If a TOC error occurs, the TOC LED turns red, but the TRACKING LED does not begin alternating. The LED will stay red until TOC is cleared or the synchronization is restarted.

3.5.2.2 TRACKING status is indicated by the TRACKING LED, which doubles as a general error indicator as mentioned above. If the tracking mode has not been reached or the station is inactive, the LED will be off. When the receiver enters the tracking mode the green half of the two-colored TRACKING LED is turned on. If the Loran-C signal is lost or if the external reference disappears (externally or internally) the TRACKING LED turns red. This will last as long as either of these conditions is true. If the Loran-C signal is lost, the receiver stops moving its tracking strobes, except to account for the "learned" frequency offset of the external reference. When the signal returns, normal tracking resumes, with the LED alternating. If the external reference is lost, the receiver stops tracking and cancels TOC. When the reference returns, the LED begins alternating. Acquisition and time synchronization will have to be restarted.

3.5.3 Besides indicating an error on the front panel, the receiver remembers that the error occured, until cleared by the operator. If an error occurs and disappears while the receiver is unattended, the operator will be aware of the problem and can decide if the error affected the timing or frequency measurement. To examine the status of the receiver, push TRACK DATA, 8. The output is a combination of eight dashes and "E's", where each character represents one of eight errors. The following paragraphs discuss the eight errors (left to right on the numeric display).

1) The left digit indicates that the receiver is in the acquisition mode when an E is displayed. Its primary function is to indicate on the IEEE-488 bus that the receiver is in the acquisition mode.

2) An E in the second digit indicates that the tracking strobe and the "fixed" 1PPS did not coincide at the correct time. On the front panel, the TOC LED will be red. This error does not cause the TRACKING LED to alternate.

3) The third position from the left indicates that a TOC synchronization has not been started or has not yet occured. When the synchronization is complete, the E is replaced with a dash. The dash remains until the TOC sequence or acquisition is restarted, or until TOC is cancelled.

4) The next error position indicates that TRACKING and TOC have been terminated, due to a loss of the external reference. This error can be caused by removing the reference from the rear panel, or by a hardware failure in the receiver. When the reference is lost, the TRACKING LED turns red and the LCD display shows the receiver status, "--EE---E", indicating not tracking,

no TOC and loss of reference. When the reference returns, the TRACKING LED begins to alternate. Acquisition and TOC will have to be restarted.

CAUTION: It will probably be necessary to reset the internal clock, if the reference is lost, before doing a time synchronization.

5) The next position indicates that the Loran-C signal is blinking or was blinked. At the start of "blink" the front panel BLINK LED comes on setting this error position. At the end of blink the LED is turned off, the TRACKING LED continues to alternate, and this error position stays set.

6) Before the Model 2100 can begin normal tracking of the Loran-C signal, it must locate the third cycle of the pulse. To do this, the slopes between adjacent positive peaks are calculated and compared to the known shape of a Loran-C pulse. The end of the third cycle is the positive going zero crossing of the 100KHz carrier, located between two peaks for which the cycle number calculation produces a value of 2.5-3.5. The variation of this number from 3.0 is due primarily to the distortion of the pulse as it propagates through the natural bandpass filter between the transmitter and receiver. The distortion is caused by the unequal delay of the various frequencies that make up a Loran-C pulse. When the Model 2100 enters the TRACKING mode, the current cycle number is saved as the "nominal" value. A variation of the cycle number exceeding ±0.5 causes a cycle error. The cycle LED is turned on and the TRACKING LED begins to alternate. A cycle error does not necessarily indicate that the receiver is tracking the wrong cycle. However, if the error continues, the receiver may have settled on the wrong cycle or may have skipped cycles.

7) When the receiver enters the TRACKING mode, the gain is saved as a "nominal" gain. If the receiver gain changes by at least ±10 dB, first order tracking of the Loran-C pulse is stopped. The second order correction, which is the frequency offset of the local reference, is still applied to the tracking strobes. The TRACKING LED turns red and the seventh indicator is set to "E". When the signal returns to normal, the TRACKING LED begins to alternate, indicating an error.

8) This indicator is set to "E" until the receiver enters the TRACKING mode, at which time it is changed to a dash. The dash remains until tracking is stopped or until acquisition is restarted.

3.5.4 To clear the error indicator, enter 0 TRACK DATA 8. If the error condition no longer exists the "E" will be replaced by a dash and the TRACKING LED turns green. If the error is still valid, the "E" will reappear within one second and the TRACKING LED continues to alternate. All errors, except for 3 and 8, are cleared (set to a dash) when acquisition is started or when normal tracking is stopped.

3.6 TIME SYNCHRONIZATION

3.6.1 To synchronize the Model 2100 with Universal Coordinated Time, the requirements are as follows:

A) The Model 2100 must be in the TRACKING mode.

B) A one-pulse-per-second (1PPS) that has been coarsely set to UTC must be connected to the EXT 1PPS input on the rear panel of the receiver.

C) The receiver's time-of-day must be set to the correct UTC second.

D) The first time-of-coincidence for the date the synchronization is to be performed must be entered into the receiver.

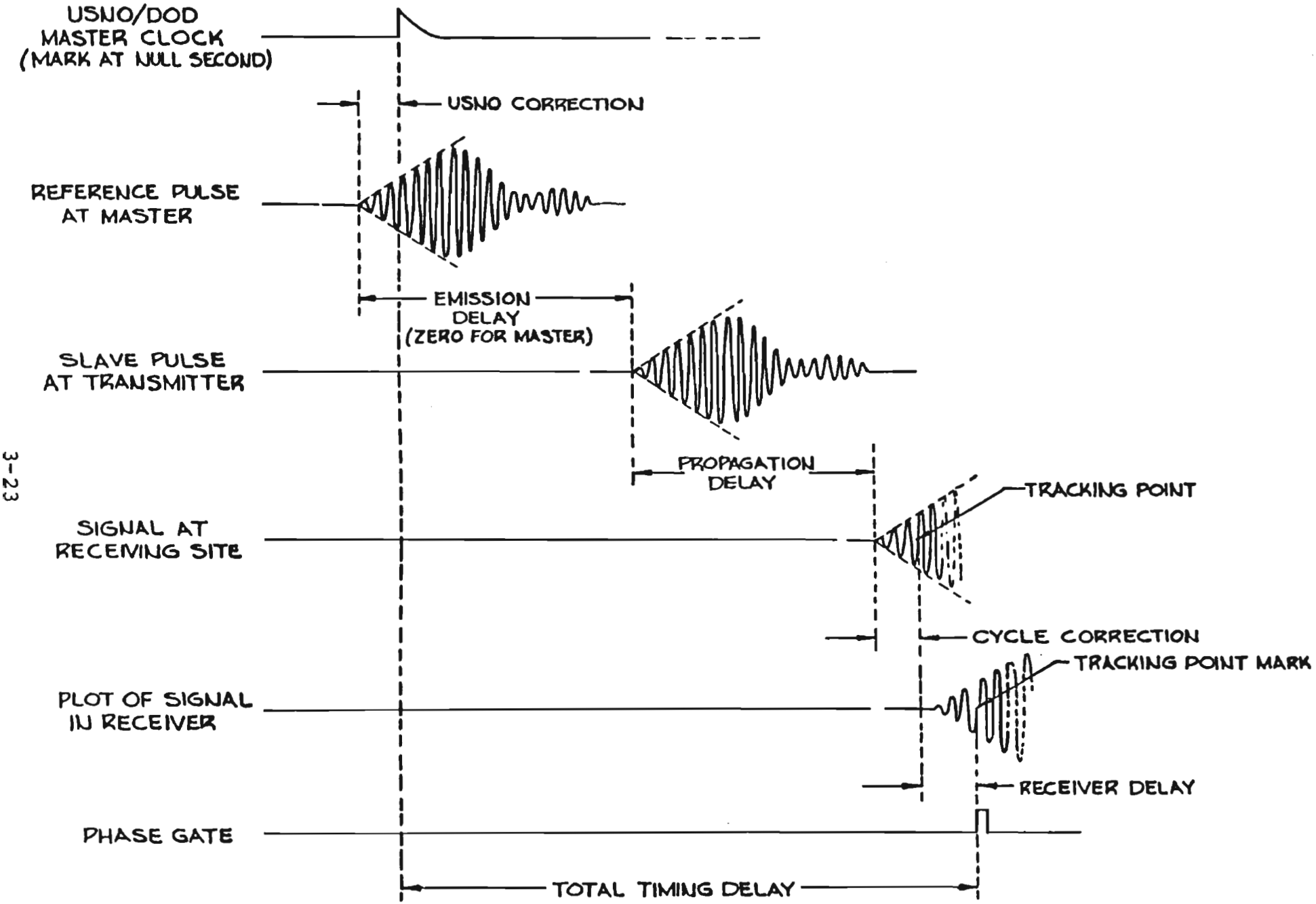
The first requirement (A) is satisfied by following the instructions in section 3.4. The remaining requirements are discussed in the following paragraphs, along with a description of Loran-C timing.

3.6.2 The Loran-C system is made up of chains of transmitters, consisting of one master station and two or more secondary stations. Each station transmits a group of 8 pulses, spaced 1 msec apart, with a carrier frequency of 100KHz. The time interval between successive transmissions of the pulse group from a station is called the Group Repetition Interval (GRI), and is the same for all stations in a particular chain. Different chains have different GRIs to minimize interference and to permit identification of the chain.

3.6.2.1 Within a chain, the order of pulse group transmissions is master first, followed by each of the secondaries. To prevent the overlap of two pulse groups from stations with the same GRI, time delays are introduced between the transmission of the master and the transmission of each of the secondaries. The order of transmission for each of the current Loran-C chains is shown in Table A-1 in the appendix.

3.6.3 Timing, using Loran-C, is accomplished by synchronizing the receiver 1PPS to the tracking point of the RF, during the GRI that is coincident with a UTC second. The normal tracking point is the zero crossing at the end of the third cycle of the 100KHz carrier, of the first pulse in the group. The resulting 1PPS is related to UTC and differs from UTC by the "Total Timing Delay" (TTD). The Total Timing Delay is the sum of the following delays. Refer to figure 3-2.

1) Antenna Coupler Delay -- This time delay includes the delay through the antenna coupler and the antenna leadin cable. It is usually on the order of 10 μsec for the AUSTRON Model 2026W Whip antenna. This delay is not shown in figure 3-2, but it must be included if timing to better than 10 μsec is required.



FACTORS IN TOTAL TIMING DELAY

FIGURE 3-2.

2) Receiver Delay -- The receiver delay is composed of amplifier delays and the delay through the 40KHz bandpass filter. It is measured at the factory and recorded on a label attached to the plastic pull tab on the 1st RF Amplifier printed circuit board.

3) Cycle Correction -- A UTC second at a time-of-coincidence is related to the start of the Loran-C pulse. Therefore, the cycle of the 100KHz carrier being tracked must be accounted for. Since the Model 2100 tracks the end of the third cycle, a correction of 30 μsec must be made. If any other cycle is being tracked, a correction, equal to the number of cycles times 10 μsec per cycle (# of cycles x 10 μsec), should be used (see section 3.7 for a discussion of cycle determination).

4) Propagation Delay -- The propagation delay is the time required for the Loran-C to travel from the transmitter to the receiver. This is the hardest correction to estimate, because the propagation speed of the Loran-C signal varies significantly as it passes over different surfaces (sea water, fresh water, dry soil, marshes, mountains, etc). An average propagation speed of 3.3413805×10^{-6} second/KM can be used which should, in most cases, give an estimated delay within ±5 μsec of the correct value provided the distance from the transmitter is known to better than about ½ kilometer.

5) Total Emission Delay -- The Total Emission Delay (TED) is the delay from the transmission of the master pulse group to the transmission of a secondary pulse group, as shown in Table A-1. For the master, this delay is zero.

6) USNO Correction -- The United States Naval Observatory

Time Service Publication, Series 4 (Daily Phase Values and Time Differences) is issued weekly, listing the observed phase and/or time differences between Loran-C stations and the USNO master clock, UTC (USNO, MC). Refer to the appendix for information on this publication.

Once the total timing delay is known, the "slewable" 1PPS in the Model 2100 can be moved earlier in time (with respect to the "fixed" 1PPS, which is synchronized to the Loran-C pulse and which will always occur after a UTC second) to produce an "on time" 1PPS.

3.6.4 Requirement B, above, states that a coarsely set 1PPS is required to do a time synchronization. The general requirement is that the 1PPS must occur before the Loran-C pulse, which was emitted during the first GRI after a time-of-coincidence, arrives at the receiver site. That is, at a time-of-coincidence, the 1PPS must occur within one GRI before the arrival of the Loran-C pulse.

3.6.4.1 An alternate approach for setting the coarse 1PPS is to set it so that it occurs within the 10 msec period ahead of UTC. If WWVB is being used, for example, synchronize the external 1PPS to the received WWVB "tic", then advance it in time by the approximate propagation time from the WWVB transmitter. This will give a 1PPS which is close to UTC. To ensure that the 1PPS occurs ahead of UTC, advance it an additional 5 msec. By doing this, the external 1PPS should occur before the Loran-C pulse arrives, even if the station tracked is a master. For a secondary, the setting of this pulse is less critical, because no secondary will be transmitted less than 10,900 μsec after a UTC second at a time-of-coincidence.

3.6.4.2 Once a suitable 1PPS is obtained, connect it to the EXT 1PPS input on the rear panel of the receiver and synchronize the "fixed" 1PPS to the external 1PPS by entering zero, then push the 1PPS SLEW function button. This function button is normally used to move the "slewable" 1PPS in time. However, to do a time synchronization these two pulses must be synchronized. The output of the 1PPS SLEW function is

the measured time interval between the occurance of the receiver "slewable" and "fixed" pulses. When the time interval is positive the "fixed" 1PPS occurs before the "slewable" 1PPS. If it is negative, the "fixed" 1PPS occurs after the "slewable" 1PPS. If the time interval is increased in either the positive or the negative direction, the sign of the time interval will change when the interval exceeds 0.5 second and the absolute value of the measurement will approach zero (with the new sign). This method of operation was chosen for two reasons:

1) there is no relationship between these two pulses beyond one second, and
2) because it can be set on time, the "slewable" 1PPS is used as the reference, with the location of the "fixed" 1PPS measured with respect to this reference (+ and -).

3.6.4.3 If an external 1PPS is not available or cannot be adjusted to the required accuracy, the "slewable" 1PPS in the Model 2100 can be used to do the TOC synchronization. Using the 1PPS SLEW function in the receiver, move the "slewable" 1PPS in time until it is set as described in section 3.6.4.1. Using a short piece of coaxial cable, connect the "slewable" 1PPS output on the rear panel of the receiver to the EXT 1PPS input. Synchronize the "fixed" 1PPS to the external 1PPS by entering zero, then push 1PPS SLEW. Leave the external 1PPS connected until the TOC synchronization is complete.

3.6.5 After connecting the coarsely on time external 1PPS to the receiver, satisfy requirement C by setting the internal 24 hour clock to UTC. To set the clock, enter a time which is several seconds in the future. When the time entered is reached, and before the next second, push the UTC function button. Verify that the internal clock agrees with the correct time.

3.6.6 To do a TOC synchronization properly, a valid time-of-coincidence, for the date of the synchronization, must be entered (Requirement D). This gives the receiver a starting point for calculating a TOC time in the future of current time. To determine the

first TOC of the day, locate the date of the synchronization, for the GRI being used, in the United States Naval Observatory Time Service Publication, Series 9 (see appendix). Enter the first TOC for that date and push FIRST TOC.

CAUTION: The receiver time is set to UTC and the first TOC of the day is UTC. When the date of the first TOC is determined, be careful to account for a date difference between local time and UTC. For example, if the time is 19:10:00 CDT on May 2nd in Austin, Texas, it is 00:10:00 UTC on May 3. Therefore, the first TOC of the day for May 3rd should be used.

3.6.7 After the four requirements are satisfied, the Model 2100 is ready to do a TOC synchronization. There is, however, one additional entry which the operator may wish to make.

3.6.7.1 If a nonzero entry for TOC ADJUST is made before a TOC synchronization, the Model 2100 will automatically slew the "slewable" 1PPS by the amount entered, after the 1PPS has been synchronized to the Loran-C at a time-of-coincidence. Normally, this number will be negative, so that after the 1PPS is slewed, it will occur earlier in time than the "fixed" 1PPS, by the total timing delay determined in section 3.6.3. If the synchronization is done correctly, the result will be a 1PPS output that is coincident with UTC, with an error equal to the error of the total timing delay calculation.

3.6.7.2 When the receiver's "fixed" 1PPS and "slewable" 1PPS are synchronized to the external 1PPS (0, 1PPS SLEW), the time difference between these pulses (as displayed by 1PPS SLEW) will be approximately +0.6 µsec. The reason for this is the difference in electronic paths within the receiver. For this reason, TOC ADJUST should be entered as the total timing delay plus the difference between the "slewable" 1PPS and the "fixed" 1PPS.

EXAMPLE:

Total Timing Delay (TTD)	=	24,572.45 µsec
1PPS Difference	=	0.54 µsec
Enter a TOC ADJUST	=	-24,572.99 µsec

3.6.8 To start the TOC synchronization process, enter 1, then push BEGIN TOC. The TOC LED begins to alternate between red and green and the numeric display shows the next TOC time (output of BEGIN TOC function button). At one second before the TOC time the receiver will respond in one of three ways:

1) If the receiver has not entered the TRACKING mode, the TOC LED continues to alternate and the next TOC time is calculated. The previous TOC time becomes the "FIRST TOC" and can be displayed by pushing, FIRST TOC. This will be repeated every TOC time until the receiver begins normal tracking.

2) If the receiver is tracking, the TOC LED will turn red. When the TOC time is reached, the LED changes from red to green, indicating that the synchronization has occured. At this TOC time, a hardware synchronization is performed. That is, the "slewable" 1PPS and "fixed" 1PPS dividers are reset to zero when the Loran-C signal arrives, after the external 1PPS occurs. The Model 2100 keeps track of future times-of-coincidence, and one-second before those times, it turns the TOC LED red. One second later (at the new TOC time) the LED turns green, if the "fixed" 1PPS and the tracking strobe (hardware pulse which occurs at the zero crossing of the 100KHz carrier of the first pulse in the group) coincide. As long as this LED is green, there was a hardware coincidence at the last TOC time. If there is no hardware coincidence, the TOC LED will remain red, indicating a possible problem. The last "good" TOC time and the TOC time when the problem was detected are saved as the FIRST TOC and BEGIN TOC outputs, respectively.

3) If the receiver is in the TRACKING mode, the LED will turn red. When the TOC time is reached (one second later), the LED stays red, indicating an error in the synchronization. It will stay red until TOC is cancelled or restarted. If this occurs, make sure the external 1PPS is connected and the internal "slewable" 1PPS and the "fixed" 1PPS have been synchronized to the external 1PPS, and start the TOC sequence again.

3.6.9 During the two or three seconds after the initial synchronization, the "slewable" 1PPS is moved in time by the amount entered through TOC ADJUST. Push 1PPS SLEW to display the time interval between the internal "slewable" 1PPS and "fixed" 1PPS and verify that it is the same as TOC ADJUST, less the initial internal 1PPS difference.

3.6.10 To determine the time interval between the external 1PPS and the "fixed" 1PPS, push TRACK DATA, 9. After a short delay, the time interval displayed will be positive (no sign) if the "fixed" 1PPS occurs ahead (early) of the external 1PPS, and negative (minus sign displayed) if the "fixed" 1PPS occurs after the external 1PPS (later).

NOTE: It is not necessary to leave the external 1PPS connected to the Model 2100 after the synchronization is complete. It is not required for subsequent TOCs. However, it must be present to measure the external-internal 1PPS time interval. If the external 1PPS is not connected, TRACK DATA, 9 will still give a number, but it will not be correct.

The interval between these two pulses will be equal to the total timing delay if the external 1PPS is synchronized to UTC. If the "slewable" 1PPS is used for the synchronization, the time difference will be the same as the 1PPS SLEW measurement, because the two pulses used are the same in both measurements, and because the "slewable" 1PPS is also synchronized to the Loran-C at a time of coincidence.

3.6.11 After a successful time synchronization, the Model 2100 keeps track of subsequent times-of-coincidence, comparing the time-of-day when a hardware coincidence occurs to the calculated next time-of-coincidence. At one second before a time-of-coincidence, the TOC LED turns red. One second later, at the time-of-coincidence, the LED turns green. As long as this LED is green, the receiver is should still be synchronized to UTC. If a hardware time-of-coincidence occurs at the wrong time, or if there is no hardware coincidence at the next time-of-coincidence, the TOC LED turns red, indicating an error. It remains red until TOC is cancelled or restarted.

3.6.12 Because of the various corrections that must be applied to do very accurate Loran-C timing, many users may wish to obtain a "clock visit". That is, a portable clock, usually derived from an atomic standard, is brought to the users' site. Using the UTC synchronized 1PPS from the clock, a TOC synchronization is done and the total timing delay, which includes all the delays discussed in this section, is determined. The delay, the GRI and name of the Loran-C station being tracked, and the date should be recorded. If time permits, two or more acquisitions and time synchronizations should be done, to verify that the receiver is consistently picking the correct cycle. In addition, it is highly recommended that this same information be determined for all Loran-C stations that can be received. These other stations can then serve as backups if the primary station is off the air for an extended period of time. If more than one receiver is located at a site, this data should be collected for those receivers, too. In other words, a "clock visit" is usually very expensive and should be used to the user's greatest advantage.

3.7 CYCLE DETERMINATION

3.7.1 Accurate time synchronization has not been accomplished when the receiver's internal 1PPS has been synchronized to Loran-C. The 1PPS obtained from the TOC synchronization is very precise, since it is derived from the phase corrected 1MHz, which is

locked to Loran-C. However, it is not very accurate, since the various delays (see section 3.6) have not been removed.

3.7.2 One delay which needs to be known accurately, to synchronize the local time to within 10 μsec of UTC, is that delay caused by the receiver tracking the third cycle of the 100KHz carrier, rather than the beginning of the pulse. The tracking point is a compromise between the no signal, time synchronized start of the pulse, and the seventh or eighth cycle, where the SNR is much better, but where skywave interference is most likely to occur.

3.7.3 It does not matter which cycle is being tracked, as long as the operator knows which cycle it is and what SNR and skywave problems may be encountered. When the Model 2100 enters the TRACKING mode it has decided that it is tracking at the end of the third cycle, which means a 30 μsec correction must be applied. If the station is within 1000 statute miles, the receiver cycle determination is very good. Beyond 1200 statute miles (ground wave signal) there may be a ±1 cycle variation in the cycle picked as the third cycle, due to the distortion of the Loran-C envelope.

3.7.4 The cycle number calculated by the receiver and displayed by TRACK DATA 5, can vary from 2.0 to 4.0 and still indicate that the receiver is on the third cycle. Before the receiver enters the TRACKING mode, it settles on a zero crossing where the calculated cycle number is 2.50 to 3.50. This allows for significant distortion of the envelope. After entering the TRACKING mode, the cycle number is allowed to vary by ±0.5, thus giving the possible range of 2.0 to 4.0. However, the cycle number will rarely exceed the 2.5-3.5 limits.

3.7.5 If the cycle being tracked is in doubt, there are two methods which may be used to determine the correct cycle. The first method is to do a TOC synchronization, account for all the delays, then compare the resulting 1PPS with an external 1PPS which is known to be accurate to within 5.0 μsec. This will usually be good enough to determine the cycle being tracked.

3.7.6 The second method is to cause the Model 2100 to scan the pulse, producing a filtered representation, which can be recorded on a linear chart recorder and analyzed by the operator. The procedure is as follows.

3.7.6.1 Before doing a scan, the receiver should have been in the TRACKING mode for at least 15 minutes. Connect a linear chart recorder to the SCAN STROBE output on the rear panel of the receiver and adjust the recorder zero to the center of the chart, with the recorder range set for 10 volts full scale. To start the scan, enter a number from 1 to 6, then push SCAN STROBE. The number entered determines the scan rate, with 1 the fastest rate and 6 the slowest rate. The fastest scan takes about 2 minutes and should give a good scan for noise numbers up to about 25. The scan time should be lengthened for higher noise numbers. The longest scan takes about 1.5 hours and should be used only when the noise number is higher than about 750. The chart recorder speed should be adjusted to give a separation between positive peaks of approximately ¼ of an inch. The following chart shows the number of GRIs sampled during the scan and the length of time required to complete the scan for each of the rates, using a GRI of 100,000 μsec. All existing Loran-C rates will require less time for a scan.

SCAN RATE	# OF GRIs	SCAN TIME
1	1,600	2.67 minutes
2	3,200	5.33 minutes
3	6,400	10.67 minutes
4	12,800	21.33 minutes
5	25,600	42.67 minutes
6	51,200	1.42 hours

3.7.6.2 When the scan is started the SCAN STROBE output on the numeric display shows the current location of the scan with respect to the third cycle tracking point, beginning at -50μsec and ending at +50μsec. When the scan reaches the tracking point, the linear output is set to zero. It remains zero for 2 μsec of scan, then continues with the

normal output. This zero period identifies the tracking point on the recording. At the end of the scan the receiver returns to normal tracking, which was suspended during the scan.

3.7.6.3 The method for determining the end of the third cycle requires that the front of the pulse be located first. Using a pencil and ruler, draw 2 straight lines on the chart record, connecting the first 4 or 5 peaks (one line through the positive peaks and one through the negative peaks). The zero-crossing of the 100KHz carrier nearest the intersection of the lines is the beginning of the first cycle. Alignment of the envelope with the carrier will not always be exact; the intersection of the envelope lines may not always occur exactly on an extrapolated zero-crossing of the carrier. Incorrect alignment of carrier cycles and envelope at the transmitter or dispersion in the propagation medium may account for the apparent misalignment. However, these effects cannot normally account for more than one-half cycle error, so that positive third cycle identification may still be accomplished easily.

3.7.6.4 After locating the start of the pulse, count back on the pulse three full cycles of the 100KHz carrier to locate the end of the third cycle. Since the Model 2100 tracks the carrier at a positive going zero crossing, the difference between the receiver tracking point and the third cycle determined above should be a multiple of full cycles of the carrier. If not, the beginning of the pulse was not correctly determined. When the correct cycle is located, count the number of cycles between the correct cycle and the receiver tracking point. If the correct cycle is to the left (earlier in time) of the receiver tracking point, enter the number of cycles to be moved (6 maximum), push the +/- key, then TRACK DATA 5. If the correct cycle is to the right (later in time) of the receiver tracking point, enter the number of cycles to be moved (6 maximum), then push TRACK DATA 5. After the tracking point is changed, the receiver will not allow an additional shift for a period of time determined by the average noise number at the time of the shift and the GRI. During this delay, the new nominal cycle number and gain are determined, which will be used to determine cycle errors and loss of signal. The following table shows the amount of delay for a GRI of 100,000 μsec and various noise numbers.

NOISE NUMBER (Range)	DELAY	# OF GRIs
≤ 4	13 seconds	128
5-8	26 seconds	256
9-16	51 seconds	512
17-32	1.7 minutes	1024
33-64	3.4 minutes	2048
65-128	6.8 minutes	4096
129-256	13.7 minutes	8192
>256	27.3 minutes	16,384

3.7.7 An alternate method for locating the end of the third cycle, involves counting half cycles of the carrier wave. This method is quite useful in high noise conditions where it can be difficult to locate the front of the pulse. However, its usefulness may be greatly limited when skywave is present.

3.7.7.1 After obtaining the pulse scan, locate the largest amplitude, positive half cycle of the carrier. This should be the seventh positive peak. Starting at the seventh peak, count backwards to tne fourth peak. The zero crossing in front of this peak (peak at 32.5 μsec) is the end of the third cycle. When the correct cycle is determined, move the receiver tracking point as described in section 3.7.6.4.

3.8 FREQUENCY MEASUREMENT

3.8.1 Another benefit of the high stability of the Loran-C groundwave and the use of cesium standards for transmissions, is the ability to make very accurate frequency comparisons. While a stationary receiver is tracking a Loran-C signal, the change in the receiver's tracking hardware to keep it on the zero crossing of the 100KHz carrier is directly proportional to the frequency difference between the transmitter's cesium standard and the local reference being used by the receiver. If the change in the receiver's tracking point (Δt) for a specific period of time (T) is known, it can be shown that,

$$\frac{\Delta f}{f} = -\frac{\Delta t}{T}$$

where $\Delta f/f$ is the relative frequency of the local frequency source. The Model 2100 keeps track of the phase shift and calculates the frequency offset automatically.

3.8.2 When the Model 2100 enters the SETTLE mode after finding the Loran-C pulse, it begins to "learn" the frequency offset of the local reference. By the time the TRACKING mode is reached, the offset has generally been determined to within a few parts in 10^9. The estimated offset can be displayed by selecting TRACK DATA 4. Shortly after starting to track, the display might be "E09 3.3, which represents an offset of 3.3 parts in 10^9. Because there is no sign in front of the number, 3.3, the frequency of the local reference is high with respect to the transmitter's cesium standard. If a minus sign is displayed, the local reference is low in frequency. As tracking continues the frequency offset calculation will gradually approach the offset of the local reference.

3.8.3 There are two factors which will influence the rate at which the frequency offset calculation approaches the final answer. These include the receiver's time constant and the signal-to-noise ratio (SNR) of the received Loran. Both of these factors also affect the stability of the calculation when the offset is better than 1 part in 10^{11}.

3.8.3.1 When the receiver power is turned on, the time constant is set to 2. This average time constant should provide good receiver response and a stable frequency offset calculation for reference offsets as low as 1 part in 10^{11} and noise numbers less than 100. Under these conditions, this accuracy should be reached in less than 2 hours. For frequency offsets lower than 1 part in 10^{11} or when the noise number exceeds 100, a time constant of one or zero should be used to provide greater averaging and to reduce the variation of the offset calculation due to noise. This will also lengthen the time for the calculations to settle.

3.8.4 Besides the automatic calculation of frequency offset, the Model 2100 also displays the total phase shift of the receiver, which can be used to manually calculate the frequency offset. The output of the 0/FS key is the total phase shift, accumulated since the receiver entered the TRACKING mode, or since the offset was reset to

zero. The advantage of this calculation is that it can be a long term average of the frequency offset, rather than the relatively short term average output by TRACK DATA 4.

3.8.4.1 When the receiver enters the TRACKING mode, the accumulated phase shift is set to zero. As tracking continues, the phase shift accumulates at a rate determined by the local reference. To calculate the frequency offset, record the phase shift and the time. Some time later, record the new phase shift and time. Divide the change in the phase shift, in seconds (multiply the displayed offset by 10^{-6}), by the time between measurements, in seconds. For example, the following data was collected:

1) TOTAL PHASE SHIFT = 0.04 = 4×10^{-8} second
TIME = 11:27:30

2) TOTAL PHASE SHIFT = 0.17 = 17×10^{-8} second
TIME = 11:47:30

CHANGE IN PHASE SHIFT (Δt) = 0.17 - 0.04 = 13×10^{-8} second
TIME BETWEEN MEASUREMENTS = 11:47:30 - 11:27:30 = 1200 sec.
FREQUENCY OFFSET = $\frac{13 \times 10^{-8} \text{ sec}}{1200} = 1.08 \times 10^{-10}$ sec

If the total phase shift at the start of the measurement is subtracted algebraically from the total phase shift at the end of the measurement, a positive result indicates that the local reference is slightly higher in frequency than the Loran-C reference. A negative result indicates a slightly lower frequency.

3.8.5 The first two methods are good for determining the average frequency offset of the local reference. However, there may be no indication of short term changes in frequency, frequency offset reversal, or abrupt phase changes. For this reason, the Model 2100 provides a voltage output, equivalent to the numeric phase shift output discussed above. A linear recorder that can take a one volt input can be connected to the PHASE RECORD output on the rear panel and a continuous record of phase changes obtained.

NOTE: The value of the voltage output may not equal the numeric output. However, the change in both outputs will be equal for the same period of time.

3.8.5.1 To use the PHASE RECORD output, connect the recorder and adjust its controls for one volt full scale, with zero along one edge of the paper. A recorder speed of 0.25 to 1 inch per hour should be adequate. To check the recorder zero, enter zero, then push 0/FS. This causes the PHASE RECORD output to go to zero volt. To check full scale, enter 1, then push 0/FS. This produces a one volt output. Adjust the recorder as necessary. Push 0/FS again to return to normal operation.

3.8.5.2 The PHASE RECORD output represents one or ten microseconds, full scale, entered through the RANGE key. When the recorder is ready, enter 1 or 10, then push RANGE. When the total phase shift reaches the range limit, the linear output returns to zero volt.

NOTE: The total phase shift shown on the numeric display does not reset at the RANGE limit as does the linear output on the rear panel. The upper limit of this number is the GRI. At that point it will reset to zero.

3.8.5.3 To determine the frequency offset from the chart record, a procedure similar to that discussed in section 3.8.4 is used. Determine the total phase shift from the record. Be careful to take the range into account. Divide the total phase shift by the period of the measurement to determine the frequency offset. If the slope of the recording is positive, the local oscillator is high in frequency. If it is negative, it is low in frequency.

3.9 ABBREVIATED ACQUISITION PROCEDURE

3.9.1 The following is an abbreviated discussion of the acquisition process, intended as a quick reference for the experienced operator. It will be assumed that the material presented in sections 3.1 through 3.5 has been read.

3.9.2 General Requirements

3.9.2.1 Antenna, properly installed and connected to the receiver.

3.9.2.2 Power, AC and/or DC, available and properly connected.

3.9.2.3 External frequency source, 1,5 or 10MHz, connected to the receiver. Toggle switch, S1, on the MPU/ Memory board set to the position corresponding to the frequency of the external reference.

3.9.3 Master Acquisition

3.9.3.1 Enter the Group Repetition Interval (GRI).

3.9.3.2 Enter 1, then push MASTER.

3.9.3.3 TRACKING mode is entered when the TRACKING LED lights.

3.9.4 Secondary Acquisition

3.9.4.1 Enter the Group Repetition Interval (GRI).

3.9.4.2 If the receiver is to select the secondary to be tracked, set SEC.TD. to zero. If a particular secondary is to be acquired, enter the appropriate SEC.TD.

3.9.4.3 Enter 1, then push SECOND.

3.9.4.4 TRACKING mode is entered when the TRACKING LED lights.

3.9.5 Receiver Status, TRACK DATA 8

3.9.5.1 Reading left to right, the indicators are:

1) Acquisition in progress.
2) TOC error. TOC stopped, TOC LED red.
3) TOC synchronization has not yet occured, or sequence has not been started.

4) TRACKING and TOC have been stopped due to loss of external reference.
5) The station is or has been blinking.
6) The cycle number is or has been out of range.
7) The tracking servos have been locked due to a loss of the RF. Normal tracking should resume when the signal returns.
8) The receiver is not yet in the TRACKING mode.

3.10 ABBREVIATED TOC PROCEDURE

3.10.1 The following is an abbreviated discussion of the time synchronization process, intended as a quick reference for the experienced operator. It will be assumed that the material presented in sections 3.6 and 3.7 has been read.

3.10.2 General Requirements

3.10.2.1 Receiver is in the TRACKING mode or will be before TOC synchronization is attempted.
3.10.2.2 EXTERNAL 1PPS input is connected to a suitable source.

3.10.3 Time Synchronization

3.10.3.1 Enter 0, then push 1PPS SLEW to synchronize the internal 1PPS to the external 1PPS.
3.10.3.2 Set internal time-of-day clock to UTC.
3.10.3.3 If the "slewable" 1PPS is to be shifted automatically after time synchronization is accomplished, enter the amount of slew (including sign), using TOC ADJUST.
3.10.3.4 Determine the first TOC of the day in the TOC tables and enter through FIRST TOC key.
3.10.3.5 Enter 1, then push BEGIN TOC to start the synchronization sequence.
3.10.3.6 Synchronization is finished when the TOC LED turns green.

4.0 IEEE-488 GENERAL PURPOSE INTERFACE BUS

4.1 SCOPE OF SECTION

4.1.1 The General Purpose Interface Bus (IEEE-488-1978) option for the Model 2100 receiver is described in this section. Included are a list of device commands and a discussion of output data formats. It is assumed that the reader is familiar with the GPIB and knows the capabilities of the controller to be used. If this option is to be installed at the customer's site, refer to the installation instructions in section 4.6.

4.2 DESCRIPTION AND SETUP

4.2.1 The General Purpose Interface Bus option for the Model 2100 Loran-C Timing Receiver is designed to operate with any bus controller that conforms to the IEEE-488-1978 specification. With appropriate software, the receiver can be programmed to acquire and track a Loran-C station. All measured or calculated data, and receiver status, presented on the front panel, are also available to the controller on the bus. Commands and data are transmitted as strings of ASCII (American Standard Code for Information Interchange) characters.

4.2.2 The Model 2100 can also be operated in the "talk only" mode. That is, in a bus arrangement where there is no controller, the receiver can be made to "talk" the data being displayed on the front panel, to a recording device, such as a line printer. New data is transmitted once a second.

4.2.3 The device capability of the Model 2100 GPIB option is shown below the IEEE-488 connector on the rear panel. These codes identify the complete set of interface functions contained within this

option. A brief discussion of each is given below. For more detail, please refer to ANSI/IEEE std. 488-1978 (IEEE Standard Digital Interface for Programmable Instrumentation).

1)	SH1 --	has complete "source handshake" capability.
2)	AH1 --	has complete "acceptor handshake" capability.
3)	T1 --	this interface can operate in the talk only mode in systems without a controller. It will also respond to a serial poll by the system controller.
4)	L2 --	this interface can operate as a basic listener; it has no listen only capability.
5)	SR1 --	can request service asynchronously from the controller in charge of the bus.
6)	RL1 --	can be programmed remotely. While in remote mode, no local programming is possible.
7)	PP0 --	has no parallel poll capability.
8)	DC0 --	has no device clear capability.
9)	DT0 --	has no device trigger capability.
10)	C0 --	cannot act as a controller.
11)	E1 --	uses open collector bus drivers.

4.2.4 To prepare the Model 2100 receiver for use on the bus, make sure receiver power is OFF and connect a GPIB cable (not supplied) to the IEEE-488 connector on the rear panel. Connect the other end of the cable to a bus controller, or to a "listen only" device such as a printer. Set the five address switches (rocker switches) to an appropriate bus address. The address switches form a five bit binary number, where the right-hand switch is the least significant bit.

NOTE: When the address of the Model 2100 is changed, power must be cycled to enter the new address.

4.2.5 The second rocker switch from the left selects ADDRESSABLE (0) or TALK ONLY (1). If the receiver is to be used with a controller, select ADDRESSABLE. If no controller is present select TALK ONLY.

4.2.6 The left-hand switch is used to enable or disable the service request feature of the bus interface (see section 4.5). Set this switch in the appropriate position.

4.3 DEVICE COMMANDS

4.3.1 Programming the Model 2100 receiver by way of the GPIB is very similar to programming from the front panel. Data is entered by depressing the appropriate numeric keys, then a function key. Data is recalled by depressing a function key. The two main differences between front panel and GPIB data entry/recall are as follows:

1) Data programming commands are transmitted in ASCII, and
2) The function keys are represented by a two character code.

EXAMPLE: Enter GRI of 79800 microseconds.

a) Front Panel: Depress numeric keys "7, 9, 8, 0, 0" and depress function key "GRI".
b) GPIB: Transmit in ASCII "7, 9, 8, 0, 0, A, 3".

EXAMPLE: Output GRI.

a) Front Panel: Depress function key "GRI".

b) GPIB: Transmit in ASCII "A, 3, M, 5". When M5 is received by the receiver, it will begin to transmit the data requested, as soon as it is made a talker. If M5 is not used, only the front panel display is changed.

4.3.2 The GPIB representation for each of the function switches on the front panel of the Model 2100 is given below, along with a brief description. The DATA FORMAT column refers to one of four formats for data put on the bus by the Model 2100. See section 4.4 for a description of these formats. For a more complete description of the function switches, refer to section 3.0.

GPIB CODE	FUNCTION	DATA FORMAT	DESCRIPTION
A0	SECOND	1	This command is used to start or stop acquisition of a secondary station. Data displayed is the approximate time-of-arrival difference between the master and the secondary.
A1	MASTER	1	This command is used to start or stop acquisition of the master. Data displayed is zero if the function is active and, "--------" if it is inactive.
A2	SEC.TD.	1	Enter and display the approximate time-of-arrival difference for the specified secondary.
A3	GRI	1	Enter and display the Group Repetition Interval (GRI) of the Loran-C station to be acquired.

F0	0/FS	1	Used to calibrate the external linear recorder for zero and full scale. Output is zero or one during calibration, and the accumulated phase shift while the station is being tracked.
F1	RANGE	1	Input/Output phase record range.
M0	CLEAR	--------	Clear numeric entry.
M1	TEST	--------	Controls operation of test routines.
M2	SCAN STROBE	1	Used to start or stop scan of Loran-C pulse. Output is the current location of the strobe with respect to the current tracking point.
M3	TRACK DATA	-,-,1,1,2 1,1,1,3,1	Input/Output various data.
M4	BACKLIGHT	--------	Turn display backlight on.
M5	*****	--------	Causes output of data to the GPIB.
T0	BEGIN TOC	4	Used to start or stop the time-of-coincidence sequence. Output is the time of the next coincidence.
T1	FIRST TOC	4	The first TOC of the day is entered using this command. Output is the time entered or the last time-of-coincidence if the TOC sequence has been started.

T2	TOC ADJUST	1	Input/Output of correction to be applied to slewable 1PPS after first time-of-coincidence.
T3	UTC	4	Enter and display the time-of-day (Universal Coordinated Time).
T4	1PPS SLEW	1	This command is used to synchronize the two receiver one-pulse-per-second outputs to an external one-pulse-per-second, to move the "slewable" 1PPS in time, and to display the time difference between the receiver "fixed" 1PPS and the receiver "slewable" 1PPS.

******** = no front panel key
-------- = no output.

4.3.3 Three examples of how these commands can be used are shown below. In the first example the GRI, the time constant, and the MASTER command are entered as a single ASCII string, which is acceptable, since the Model 2100 processes each character before accepting another. In some controllers, however, the number of characters in a string, that can be output by a single controller command, may be limited. If this is true, it is recommended that programming data for the receiver be sent as separate ASCII strings consisting of the numeric data followed by the 2 character code for the receiver function being programmed. Therefore, an alternate form of Example 1 is:

```
Output ASCII string "99600A3" (GRI)
Output ASCII string "4M36"    (time constant)
Output ASCII string "1A1"     (start acquisition)
```

NOTE: Quotation marks are used here to indicate the ASCII string and should not be transmitted to the Model 2100.

4.3.3.1 EXAMPLE 1: Enter a GRI of 99600 microseconds, enter a time constant of 4, and start acquisition of the master.

Output ASCII string "99600A34M361A1"

EXAMPLE 2: Enter the approximate time difference for a secondary and start acquisition.
Assume a secondary TD of 36000 usec.

Output the ASCII string "36000A21A0"

EXAMPLE 3: Set internal time-of-day clock and output on the bus (for example TOD = 15:30:00).

Output ASCII string "153000T3M5"

4.4 DATA FORMAT

4.4.1 All data and status information displayed on the front panel of the Model 2100 can be transmitted on the bus by sending the two digit code of the function (data) to be output, followed by the code, "S4". (If the data required is already being output to the front panel display, transmission of "S4" is sufficient.) After sending, "S4", the controller must make the receiver interface a "talker" for the requested data to be sent.

4.4.2 There are 4 data formats used by the Model 2100 receiver to send data on the bus. The format for each function key on the front panel is shown in Section 4.3.2. The format for each STATUS

output is indicated in the same order the data is presented. In all cases, the data output consists of a string of twelve ASCII characters, which includes some combination of numbers, letters, colons, spaces (sp), a decimal point (DP), a minus sign, and a carriage return (CR) and line feed (LF). The order of transmission is from left to right as shown below. If the data requested is not yet available, dashes (-) will be transmitted. When the line feed (LF) is sent, the End or Identify (EOI) interface line is made active low to indicate that the last byte of the string is being sent. Many controllers (or listeners) accept the ASCII combination of carriage return and line feed as the end of a data transmission and do not monitor EOI. These devices should experience no problems with the receiver output. For devices that monitor EOI, it may be necessary to remove the carriage return and line feed bytes before using the data.

4.4.2.1 The first and most common data format is that used to output GRI. This data consists of:

(sign)(6 digits)(DP)(2 digits)(CR)(LF)

If the sign of the data is negative, an ASCII "-" is transmitted. If the data is positive, an ASCII "space" is transmitted.

FORMAT 1: a GRI of 79800 is sent as,
(sp)079800.00(CR)(LF),
a gain of 87 is sent as,
(sp)000087.00(CR)(LF).

4.4.2.2 The second format type is that used for the calculated frequency offset. This data consists of:

(sp)(sp)(sp)(sign)(1 digit)(DP)(1 digit)(ASCII "E")(2 digits)(CR)(LF)

The first digit sent, the decimal point, and the second digit represent the mantissa of the frequency offset. The ASCII "E" and the last 2 digits represent the exponent of the frequency offset.

FORMAT 2: A frequency offset of -4.8×10^{11} issentas,(sp)(sp)(sp)-4.8E11(CR)(LF)

4.4.2.3 The third format type is that used to send acquisition and track status. This consists of:

(2 spaces)(8 digits, ones and zeros)(CR)(LF)

Each digit represents a true condition (1) or a false condition (0) for each status type. Refer to section 3.0 for a description of each status byte. Note that the front panel display shows "-" (dashes) for a false status condition and "E" for a true status condition.

FORMAT 3: Status indicating NOT TRACKING is sent as, (sp)(sp)00100001(CR)(LF)
Status indicating REFERENCE LOSS is sent as (sp)(sp)00110001(CR)(LF)

4.4.2.4 The last format type is that used for time. The format is:

(2 spaces)(Hours)(colon)(Minutes)(colon)(Seconds)(CR)(LF)

FORMAT 4: The time of day, 15:30:27, is sent as (SP)(SP)15:30:27(CR)(LF).

4.5 SERVICE REQUEST

4.5.1 The status of the Model 2100 can be monitored continuously on the bus by reading TRACK DATA 8. However, a more efficient process is to monitor the GPIB SRQ (Service Request) bit. In the 2100, the SRQ bit is set active (LOW) when one of the bits in the status word becomes true (except for the acquisition-in-progress bit) or when there is a keyin error. When this occurs, the controller conducts a Serial Poll to obtain the service request information.

4.5.2 The service request information tells the controller what kind of service is required. The bit assignment for this information is given below:

a) Bit 0 = Switch keyin error
b) Bit 1 = NOT ASSIGNED
c) Bit 2 = Receiver tracking error
d) Bit 3 = Loss of external reference
e) Bit 4 = NOT ASSIGNED
f) Bit 5 = NOT ASSIGNED
g) Bit 6 = IEEE-488 assigned as DEVICE SERVICE REQUEST
h) Bit 7 = NOT ASSIGNED

4.5.2.1 Bit 0 indicates that there has been an improper keyin. A keyin error will occur if a keyin sequence is in error (i.e., for the TRACK DATA key) or if the data entered is out of range. The correct response is to send CLEAR (M0), because no other keyin will be allowed until the error is cleared.

4.5.2.2 Bit 2 is set when a condition exists which may affect normal Loran-C tracking. These conditions include BLINK, CYCLE ERROR, and loss of signal, which generate a service request when they begin and end. The controller should read TRACK DATA 8 to determine the condition which caused the service request.

4.5.2.3 Bit 3 is set when the external reference is lost of if it is interupted for longer than about 100 μsec.

4.6 IEEE-488 OPTION INSTALLATION

4.6.1 The following paragraphs describe the proper procedure for installing the IEEE-488 option in the Model 2100 Loran-C Timing Receiver (if the option was ordered at the same time as the receiver, this section may be skipped). The only tools required are a flat blade screwdriver, a #1 Phillips screwdriver, and a 9/32 inch nut driver or wrench.

4.6.2 Set the power switch to the OFF position and disconnect the AC and DC power cords. Using the flat blade screwdriver, remove the top cover. Mounted on the inside surface of the rear panel is a plate covering two rectangular holes. Remove this plate.

4.6.3 Secure the IEEE-488 interface circuit board (AUSTRON P/N 10398250) to the inside surface of the rear panel, as shown in figure 4-1, using the mounting hardware provided. Once the lockwashers and nuts are in place, tighten the standoffs with the nut driver while holding the nuts.

4.6.4 While supporting the IEEE-488 interface board from below, connect one end of the cable (AUSTRON P/N 12098095) to the 26 pin connector. Be careful to align the arrow on the cable connector with the arrow on the board, as shown in figure 4-1. Attach the other end of the cable to the 26 pin connector on the interconnect board, being careful to align the arrows on the connector and the interconnect board.

4.6.5 Install the top cover and reconnect the power cable(s). Before turning the receiver power on, review paragraph 3.1.2 of the OPERATING INSTRUCTIONS. When power is applied the Model 2100 should respond as described in that section.

4.6.6 If the receiver does not respond as expected, turn power off immediately. Disconnect the power cable(s) and remove the top cover. Make sure the ribbon cable has been installed correctly, with the alignment arrows on the cable connectors opposite those on the two boards. If one of the connectors is backwards, one of the fuses on the rear panel may have been blown. After correcting the problem, replace the cover and reconnect the power cable(s). Turn power on and verify proper operation.

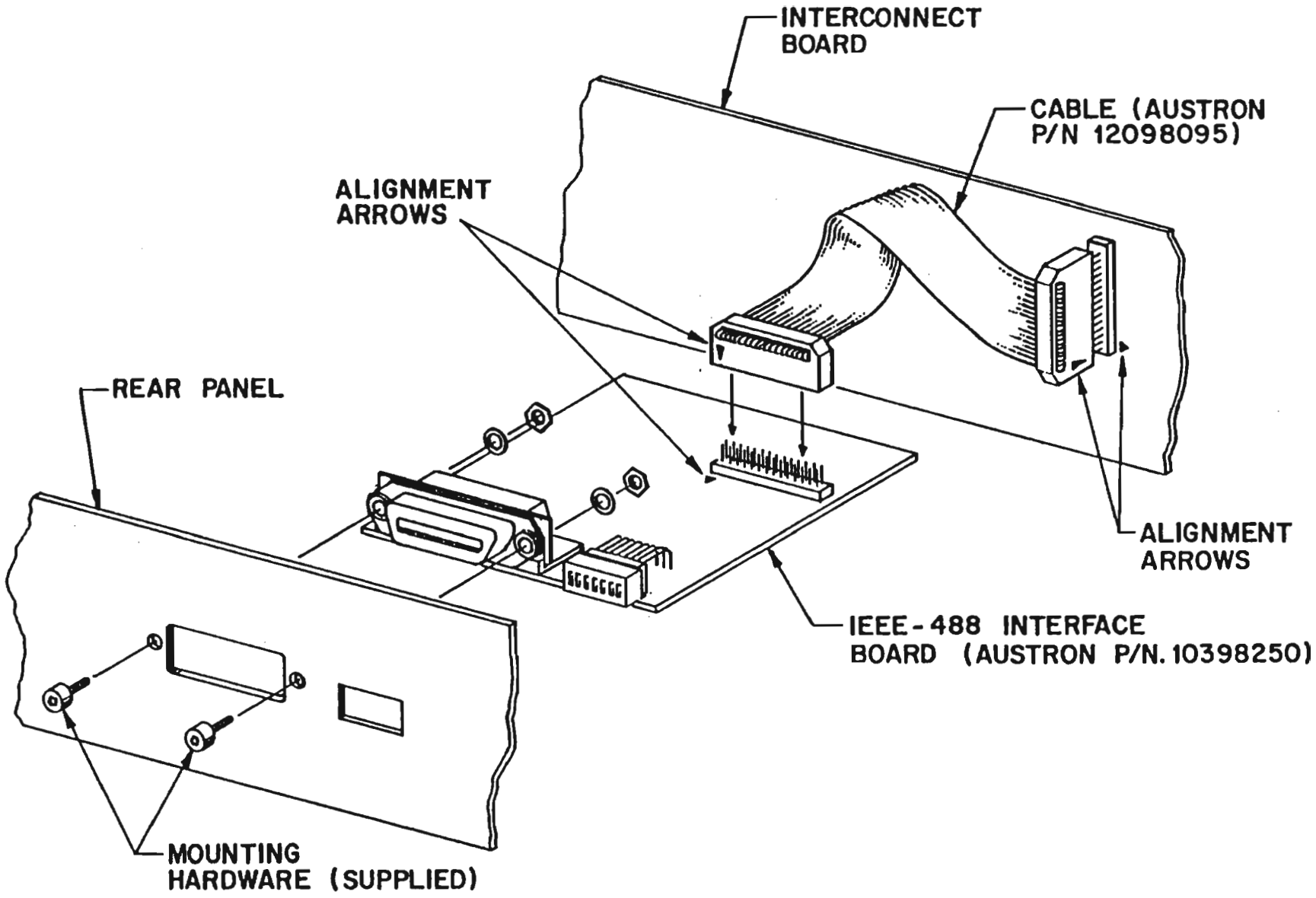


Figure 4-1. IEEE-488 Interface Installation (Option-01)

5.0 CIRCUIT DESCRIPTION

5.1 SCOPE OF SECTION

5.1.1 This section provides a circuit analysis for the AUSTRON Model 2100 Loran-C Timing Receiver. Included are schematics, assembly drawings and detailed descriptions of the circuits. Generally, signals are traced from left to right on the schematics. When referring to the digital circuitry, a high level (2.4V to 5V) is a logical one and a low level (0V to 0.8V) is a logical zero.

5.2 CIRCUIT ANALYSIS

5.2.1 1st RF Amplifier (Reference Designator 1A1A2A1, Figures 5-1 and 5-2). The 1st RF Amplifier amplifies and filters the antenna input. There are also four attenuator stages which permit microprocessor control of the receiver gain. The 50 ohm (RG-58) antenna leadin is coupled to the first amplifier stage by the impedance matching transformer, T1. T1 also provides approximately 20 dB of gain. The signal is then amplified by 16 dB in U1 and U2 and by 8 dB in U3. From U3, the signal passes through a 5 pole Bessel filter, which has a center frequency of 100KHz and a bandwidth of 40KHz. Additional amplification is provided in U4, U5 and U6 before the signal leaves the 1st RF amplifier.

5.2.1.1 U7 consists of 4 single pole, single throw analog switches, which are used to control the gain of the 1st RF amplifier. Since the operation of each switch is the same, only U7B will be discussed. The signal at the output of U1 goes through R6 to the noninventing input of U2. R6 and R10 form a voltage divider when the control voltage to U7B pin 8 goes to ground, closing switch U7B. This causes a 32 dB attenuation of the signal.

5.2.2 2nd RF Amplifier (Reference Designator 1A1A2A2, Figures 5-3 and 5-4). U1 through U4 form a four stage amplifier with a total gain of 38 dB. U7 consists of four single pole, single throw analog switches used in four microprocessor controlled attenuators (see section 5.2.1.1).

5.2.2.1 The output of amplifier U2 goes to buffer U5 which drives the 3 pole Butterworth filter. The output of the filter is converted to a TTL level signal by U6. The output of U6 is the hard limited RF used for acquisition.

5.2.2.2 The output of U4 is the amplified and filtered Loran-C signal.

5.2.3 A/D Converter (Reference Designator 1A1A2A3, Figures 5-5 and 5-6). The amplified signal from the 2nd RF Amplifier is connected in parallel to 3 track-and-holds, U6, U12 and U13. When the receiver is tracking a Loran signal this board is active and the following sequence is repeated eight times every GRI.

5.2.3.1 The sequence is started when WINDOW goes high, enabling U3. WINDOW also enables gates U1-A, B and C allowing the CYCLE, PHASE, and AMPLITUDE pulses to pass through and put their respective track-and-hold amplifiers in the "hold" state. Each track-and-hold samples a different place on the Loran pulse for use in tracking. When AMP HOLD goes high, oneshot, U3, produces a short pulse which clears shift register, U5, and generates a CONVERT pulse to the A/D converter, U9, converting to binary the voltage in track-and-hold, U13. When done, U9 generates the microprocessor unit (MPU) interrupt, A/D $\overline{\text{IRQ}}$. The MPU reads the upper byte of U9 by enabling the buffer, U10. The same read pulse clocks the shift register, U5, selecting the AMP HOLD track-and-hold through analog multiplexer, U2. The MPU then reads the low byte by enabling buffer U11. This pulse also triggers U3, producing the next CONVERT command to U9. This process repeats for the AMP HOLD and CYCLE HOLD samples. When the high byte of the CYCLE HOLD sample is read, U5 is

clocked the third time, causing U5 pin 14 to go low, disabling gate U4-B and stopping further CONVERT pulses. This cycle is repeated for each Loran pulse (8 times for a secondary and 10 times for a master).

5.2.3.2 IC U7 adds together the RF from the 2nd RF pcb and the step pulse. This composite signal is inverted and buffered by U8 to provide the oscilloscope vertical output on the rear panel.

5.2.4 1MHz Phase Shifter (Reference Designator 1A1A2A4, Figures 5-7 and 5-8). The 1MHz Phase Shifter pcb produces the phase shifted 1MHz used for tracking, the phase corrected 1MHz and 10MHz signals for the rear panel, and the "slewable" 1PPS.

5.2.4.1 The buffered external reference (reduced to 1MHz on the MPU/MEMORY pcb if a 5MHz or 10MHz reference is used) is divided by U37 to 500KHz. This signal serves as reference to two nearly identical digital/analog phase shifters. The Main Phase Shifter, under program control, phase shifts the 500KHz, which is then doubled to 1MHz by Doubler B. The 1MHz output of Doubler B is the reference for the tracking hardware which produces the Loran signal sampling strobes.

5.2.4.2 The Auxilliary Phase Shifter uses the digital-to-analog converters output (U29) to produce a phase shifted 500KHz identical to the 500KHz generated by the Main Phase Shifter. Normally, the track-and-hold IC, U41, tracks the output of U29. When the total phase shift changes from 0.99 µsec of 0.00 µsec or from 00.0 µsec to 0.99 µsec, U41 goes into the hold mode, maintaining the last phase shift. The input to Doubler A (U3A pin 1), which most of the time uses the phase shifted output of the Main Phase Shifter, is also switched to the output of the Auxilliary Phase Shifter. The Main Phase Shifter is then set to the new phase shift (0.00 or 0.99). After approximately 200 µsec, the Auxilliary Phase Shifter is switched out and the Main Phase Shifter is switched in. This process produces a smoothly phase shifted 1MHz at the output of Doubler A.

5.2.4.3 The 10MHz Phase Locked Loop is locked to the phase shifted output of Doubler A to produce a 10MHz output locked to the Loran-C signal being tracked. Doubler A also provides the reference for the 1 PPS Divider which produces the 1 PPS interrupt for the firmware time-of-day clock.

5.2.4.4 The RF Gain Control Register is loaded by the MPU with an 8 bit binary number representing the current receiver gain. The eight outputs of this register enable and disable the attenuators on the 1st and 2nd RF pcbs to maintain a constant RF output.

5.2.4.5 The Register Selector (U40) is a 4-line-to-16-line demultiplexer which produces pulses to control the various registers on this pcb.

5.2.4.6 The 1PPS MASK REGISTER is used to move the "slewable" 1PPS in time, in response to operator inputs. The 24 bit comparator (U7, U16 and U27) compares the contents of the 24 bit counter (U6, U15, and U26) to the contents of the 24 bit latch (U8, U17, and U28). When the 1PPS is not being slewed, the latch is loaded with the binary equivalent of 999,999. To move the 1PPS earlier in time, the latch is loaded with a number less than 999,999 by the amount of the slew. To move the 1PPS later in time, the latch is loaded with a number greater than 999,999, by the amount of the slew. When the latch and counter are equal, the output of the comparator, U27 pin 19, goes low enabling flip flop, U22A, in the 1PPS PHASE SHIFTER. On the next positive going edge of the phase corrected 1MHz, the Q output of U22A goes low, clearing the 1PPS MASK REGISTER divider, through gate, U32C. At the same time, the $\overline{Q}$ output of U22A goes high, triggering one-shot, U20A. The 1PPS PHASE SHIFTER delays the output of U22A by the fraction of a microsecond specified by the operator. The Q output of one-shot, U36B, is the phase shifted 1PPS.

5.2.4.7 The 1PPS PHASE SHIFTER produces the "fraction-of-a-microsecond" phase shift of the "slewable" 1PPS. Digital-to-analog converter (DAC), U18, converts the binary input to a voltage.

Integrator, U19, and one-shot, U20B, are connected together to produce a linear change in the period of the one-shot, in response to the linear output of the DAC. The DAC and integrator can shift the incoming 1MHz by approximately 0.49 microsecond. For phase shifts greater than 0.49 microsecond, the 1MHz is inverted by U11C (controlled by latch, U37A). With the DAC set to zero, this produces a 0.5 microsecond shift. As the DAC voltage increases, the amount of phase shift increases to approximately 0.99 microsecond.

5.2.5 Acquire/Track (Reference Designator 1A1A2A5, Figures 5-9 and 5-10). For acquisition and track, it is necessary to produce a strobe every GRI which initiates sample taking. In the Model 2100, this is accomplished by dividing the external reference down to the repetition rate of the Loran signal.

5.2.5.1 The Mask Match Divider is a 25 bit free-running binary divider. As the divider counts, the contents of the lower 17 bits are compared by the Mask Match Latch. When counter and latch match, the comparator output, U45 pin 19, goes low. The next positive going edge of the phase shifted reference, 1MHz(A), causes the Mask Match Output, U18A pin 6, to go high, setting U15B. This causes a microprocessor interrupt request ($\overline{\text{IRQ}}$). The contents of the counter at the next GRI interrupt is then calculated in the software and output to the Mask Match Latch. During this calculation, the 24 bit Mask Match Register is loaded and read by the software to verify the current count. This process continues as long as power is on.

5.2.5.2 The Mask Match Output occurs approximately 950 usec before the arrival of the Loran pulses. This allows time for two things to occur. First, the RF Gain Control Register on the 1MHz Phase Shifter pcb is loaded with the new gain to be used during the sample taking. Second, the Acquire/Track Divider and the Tracking Strobes Generator are initialized.

5.2.5.3 During the first microsecond after Mask Match, U21A pin 5 is high, resetting the Acquire/Track Divider. When U21A pin 5 goes

low, the divider begins to count. After about 950 usec, WINDOW is generated, followed by TRIGGER. The trigger pulse occurs 40 usec before the normal tracking point.

5.2.5.4 At 32.5 usec after TRIGGER, the CYCLE HOLD strobe is generated, followed 7.5 usec later by PHASE HOLD and 10 usec later by AMP HOLD. These three strobes control the TRACK/HOLD circuits as discussed in section 5.2.3, and are repeated 8 times (1 msec apart) if the Loran-C station is a secondary and 10 times for a master. The WINDOW and TRIGGER pulses last 7.5 msec for a secondary and 9.5 msec for a master.

5.2.5.5 During acquisition, the software is synchronized to the Loran-C signal by recording the occurrence of mask match in Shift Register B. After synchronization, hard limited (TTL compatible representation of the RF signal, 1 = positive Rf voltage and 0 = zero or negative RF voltage) RF samples are taken from Shift Register A via the tristate buffer, U38. These samples are used to determine the location of the Loran-C signals.

5.2.5.6 When service is required by one of the devices in the Model 2100, it sets one of the bits in the $\overline{\text{IRQ}}$ Register. The register consists of 4 dual flip-flops, U14, U15, U16, and U17. When a bit is set, the output of U10A goes low, generating the $\overline{\text{IRQ}}$. The MPU reads the register through buffer U30, then outputs what it read to U29. The outputs of this inverting buffer reset the corresponding flip-flops in the $\overline{\text{IRQ}}$ Register, if that flip-flop was set when the register was read. In this way, additional interrupts will not be reset if they occur during the reset cycle. The Receiver Mask makes it possible for the software to inhibit certain interrupts when they might interfere with a calculation.

5.2.5.7 The Analog Phase Shift Buffer converts the binary phase shift from the MPU into a voltage that ranges from 0 to 1 volt full scale. U28 pin 18 goes to the PHASE RECORD output on the rear panel.

5.2.5.8 U48 is a 4-line-to-16-line demultiplexer which decodes the MPU address bus to select one of the registers on this printed circuit board. When active, an output is low for 0.5 usec.

5.2.5.9 The SCAN STROBE output is the averaged Loran-C pulse, resulting from the scan. The microprocessor samples the Loran-C pulse at regular intervals, for several GRIs at each sampling point. The averaged result for each point is output to the latches, U31 and U32. These latches control the 12 bit, bipolar DAC, U43, which drives the external linear recorder.

5.2.5.10 DAC, U41, integrator, U42, and one-shot, U40B, form a microprocessor controlled, linear phase shifter, used to provide submicrosecond sampling of the Loran-C pulse during scan. This phase shifter works as described in section 5.2.4.7.

5.2.6 MPU/MEMORY (Reference Designator 1A1A2A6, Figures 5-11 and 5-12). The MPU/MEMORY printed circuit board is the main controller for the 2100. The control program, contained in 3 erasable-programmable-read-only-memory (EPROM) integrated circuits, is located on this board along with the microprocessor, random access memory (RAM, used for temporary data storage), and address and data bus buffers.

5.2.6.1 The microprocessor, U3, executes the program contained in the three EPROMs, U41, U42, and U43. The RAM/EPROM Address Decoder selects one of the EPROMs, depending upon which part of the program is being executed. The program bytes go to the MPU via Interface B. The RAM consists of U25, U26, U27, and U28 and is organized as 2048 locations, 8 bits wide. Each integrated circuit is organized as 1024 locations, 4 bits wide, so that two ICs are required for each 1024 locations. The RAM serves as temporary storage for the MPU and uses Interface B to buffer data transfers between itself and the MPU.

5.2.6.2 Interface C buffers the address lines from the microprocessor. The 16 buffered address lines are used on this board

and are available on the receiver interconnect board.

5.2.6.3 Interface A is an 8 bit bidirectional interface which buffers the low drive outputs of the MPU to the main data bus in the receiver. The buffer is active when U38 pin 19 is low. The direction of data flow is controlled by the MPU read write line ($\overline{R/W}$). This signal is connected to U38 pin 1 and when high, allows data from the receiver registers to be read by the MPU. When low, the MPU is writing to the receiver registers. When switch S1 is in the TEST position, Interface A is disabled.

5.2.6.4 The Front Panel Interface is the buffer between the front panel switches and displays, and the MPU. When pin 19 of U37 is low, the bidirectional buffer is enabled and data passes between the MPU and the front panel. When data is loaded into or read from registers on the front panel, 0.5 usec strobes from the 3-line-to-8-line demultiplexer, U12, enable the appropriate registers.

5.2.6.5 The external reference is shaped and buffered by transistors, Q1 and Q2, and divided by U8, if necessary, to produce the 1MHz reference used by the receiver. Switch S1 is set to the frequency of the reference. Oneshot, U7, is adjusted to give a square wave output.

5.2.6.6 The Quadrature Clock is a derivative of the main microprocessor clock, $\emptyset 2$. Approximately 250 nsec after $\emptyset 2$ goes high, the quadrature clock, Q, goes low and returns high when $\emptyset 2$ returns low. While Q is low, data on the MPU data bus is valid.

5.2.6.7 When the Model 2100 is tracking, the Carrier Relay transistor, Q3, will be off. When the servos lock due to loss of signal, Q3 will come on. If a pullup resistor is used as described in section 2, the carrier relay output will be high during track and less than 0.5 volt while the servos are locked.

5.2.6.8 The time interval counter consists of a 21 bit divider (U20, U21, and U22), a ramp-and-hold circuit (U9 and U10), counter

control circuitry (U16, U17, U18, U9, U30, and U31), and an MPU interface (U33, U34, U35, and U36). The analog-to-digital converter, U32, is used to determine the fraction of a microsecond difference between the two pulses. U18 and U19 form an MPU-controlled gate, which selects between the external 1PPS and the internal "slewable" 1PPS. The operation of this counter is as follows: The internal "fixed" 1PPS always is the start pulse, clocking the "start" flip flop, U16 pin 3, on the positive going edge. U16 enables the "stop" flip flop, U30 pin 2, and the 1MHz control flip flop, U16 pin 12, 13. On the next positive going edge of the 1MHz clock, U16 pin 9 goes high, enabling gate, U17. This applies clock pulses to the 21 bit divider, counting whole microseconds. When the "stop" pulse occurs, U30 pin 5 goes high, enabling U30 pin 12 and starting the ramp generator, U10. On the first positive edge of the 1MHz, after the stop pulse, U30 pin 9 goes high, enabling U31 pin 12. On the second edge, U31 pin 9 goes high enabling U31 pin 2 and setting the hold circuit, U9, to the hold state. This saves the voltage of the ramp at that moment. The output of the hold circuit is buffered and amplified by U1. The resulting voltage goes to the A/D converter and is proportional to the frational part of the time interval. At this point in the measurement, the divider contains the number of whole microseconds. On the third edge, U31 pin 6 goes low, starting the A/D converter, U32. When the conversion is through, U32 pin 17 goes low, generating an MPU interrupt. The MPU responds to the $\overline{IRQ}$ by latching the contents of the divider in the MPU buffer (U33, U34, U35, U36) and enables the counter for another measurement. The MPU then reads the measurement and corrects it for the extra counts accumulated during the ramp.

5.2.7 +5V SWITCH REGULATOR (Reference Designator 1A1A2A7, Figures 5-13 and 5-14). The main power supply in the Model 2100 is the +5 volt switching regulator. It supplies the +5 volt power for all the logic circuits and the +5V to ±12V converter on the receiver backplane. U1 samples the output voltage and changes the "ON" time of power transistor Q1 to maintain +5 volts. Inductor L1 and capacitor C6 filter the pulses from Q1 to give a dc output. U3 samples the output voltage and switches on if it exceeds 6.8 volts. This will cause either the DC or

AC fuse on the rear panel to open, turning off the receiver and protecting the logic circuits from the excessive voltage. U2 converts the +5 volts to a 60 volt ac voltage at 400Hz to power the liquid crystal display backlight.

5.2.8 FRONT PANEL LCD DISPLAY/KEYBOARD (Reference Designator 1A1A1, Figures 5-15 and 5-16). Programming information and calculated data are entered and displayed through the front panel. The numeric display is an eight digit liquid crystal display. The MPU loads the numeric data into display controllers, U7 and U8, which produce the necessary signals to control the display.

5.2.8.1 Receiver status is indicated by several LEDs, driven by latches, U2 and U3. Three of the outputs of U2 (pin 5, pin 16, and pin 19) are buffered by U1-B, U1-C, and U1-D to produce the signals, out of phase with respect to the LCD backplane, that turn on the colons, decimal point and minus sign.

5.2.8.2 Two switch encoders (U4 and U6), each capable of handling 20 switches, determine which key is pushed, generate an interrupt, then transfer a binary number representing that key, when read by the MPU. A switch encoder is read by enabling buffer, U5, at the same time the $\overline{OE}$ input of the encoder is pulled low.

5.2.9 POWER DISTRIBUTION AND INTERCONNECT (Reference Designator 1A1A2, Figure 5-17 and 5-18). The interconnect board provides the necessary connections between the printed circuit boards in the receiver. The interconnections are such that the 3 large digital boards can be plugged into any position, making it possible to test a board by placing it in the top slot. For normal operation, the preferred order is:

TOP	=	1MHz PHASE SHIFTER
MIDDLE	=	ACQUIRE/TRACK
BOTTOM	=	MPU/MEMORY

In the RF section, the 1st and 2nd RF Amplifier circuit boards may be installed in either of the top 2 slots. For normal operation, the 2nd RF Amplifier should be inserted in the top position, with the 1st RF Amplifier in the middle position. The A/D Converter must always be installed in the bottom slot.

5.2.9.1 The interconnect board also has a full wave rectifier (CR1-CR4) and filter (C1) to convert the sinewave secondary of the power transformer to the unregulated dc for the +5V regulator. A blocking diode (CR5) isolates the external dc from the unregulated dc while ac power is available.

5.2.9.2 The ±12V dc is derived from a dc-to-dc converter (U1) located on the right-hand side of the interconnect board (viewed from the front of the chassis). The converter is plugged into the interconnect board and can be replaced by removing the retainer.

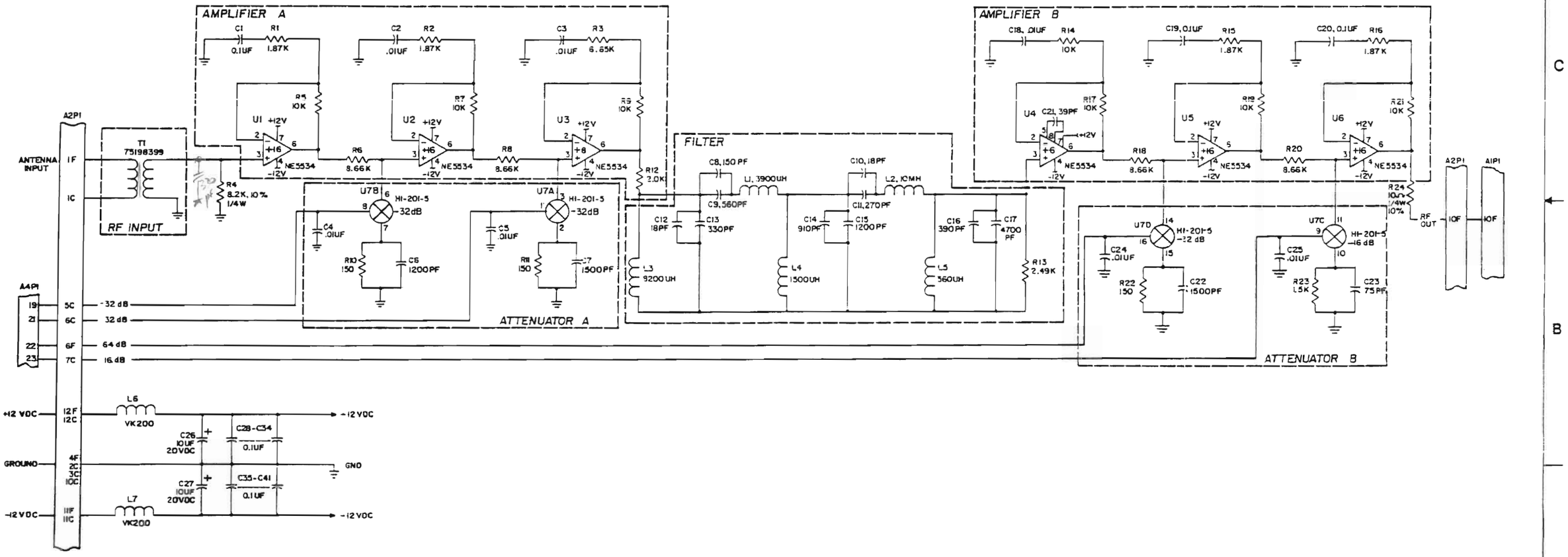
5.2.10 IEEE-488 GENERAL PURPOSE INTERFACE OPTION (Reference Designator 1A1A3, Figures 5-19 and 5-20). The General Purpose Interface permits connection of the Model 2100 to the General Purpose Interface Bus (IEEE-488-1978 specification). Buffer ICs, U3 and U5, are connected directly to the bus and provide the drive and isolation characteristics required by the specification. U2 is the main interface IC. Data from the receiver MPU and from the bus, pass through U2. U2 also responds to single line and multiline commands from the bus controller and provides the handshake signals necessary for data transmission.

5.2.10.1 Switch, S1, is loaded by the operator with the bus address of the Model 2100. The MPU reads this switch through Switch Buffer, U7, when U7 pins 1 and 19 are low. S1 also contains the MPU instructions for SRQ or NO SRQ, and ADDRESSABLE or TALK ONLY.

5.2.10.2 The Address Decoder produces the enable pulse for U2 ($\overline{CS}$) and for the Data Buffer, U4. U4 is enabled any time U2 is addressed

by the MPU, except when the Address/Control Switches are read. When this occurs, $\overline{ASE}$ (U2 pin 4) is low, enabling Switch Buffer, U7, and disabling gate, U6. This keeps U4 and U7 from driving the MPU data bus at the same time.

REVISIONS			
ZONE/LTR	DESCRIPTION	DATE	APPD



NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/8W., 1%, WITH VALUES IN OHMS

NEXT ASSY	USED ON	REF DES	FIG NO
10398067	2100	1A1A2A1	5-8
10398067	2100F	1A1A2A1	5-8

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL

ENGR
CHECKED
DRAWN SCHMIDT 11-17-80

AUSTRON INC. AUSTIN, TEXAS

SCHEMATIC, 1ST RF AMPLIFIER

SIZE 4 | CODE IDENT NO 24672 | 123 98068

SCALE N/A | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	4-15-81	

506025-0010

10398067

00398066

520400-0042
2 PLCS

25498042	2100	IAIA2AI	5-2
25498281	2100F	IAIA2AI	5-2
NEXT ASSY	USED ON	REF DES	FIG NO

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR
CHECKED
DRAWN ANE 11-25-80

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY., 1ST RF AMP

SIZE 3 | CODE IDENT NO 24672 | 103 98067

SCALE NA

SHEET 1 OF 1

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPD

AMPLIFIER

BUFFER

FILTER

3-POLE BUTTERWORTH
4KHZ BANDWIDTH
100KHZ CENTER FREQ.

COMPARATOR

ATTENUATOR

XA1 1OF → P1 1OF → RF IN

XA4 Y → 5F 8 dB

XA4 26 → 7F 4 dB
XA4 27 → 8F 2 dB
XA4 28 → 9C 1 dB
XA5-8 → 9F ML STROBE

+12VDC 12E,C → +12V
GROUND 10C, GND 4C,3C, 2C,4F 2F → GND
−12VDC 11F,C → −12V

RF OUT 3F → XA3 1C

ML OUT 8C → P1 → XA5 D

NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/8W, 1%.

10398071	2100	1A1A2A2	5-3
10398071	2100F	1A1A2A2	5-3
NEXT ASSY	USED ON	REF DES	FIG NO

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS FRACTIONS ANGLES

MATERIAL

ENG'R

CHECKED

DRAWN LDP 11-21-80 SCALE N/A

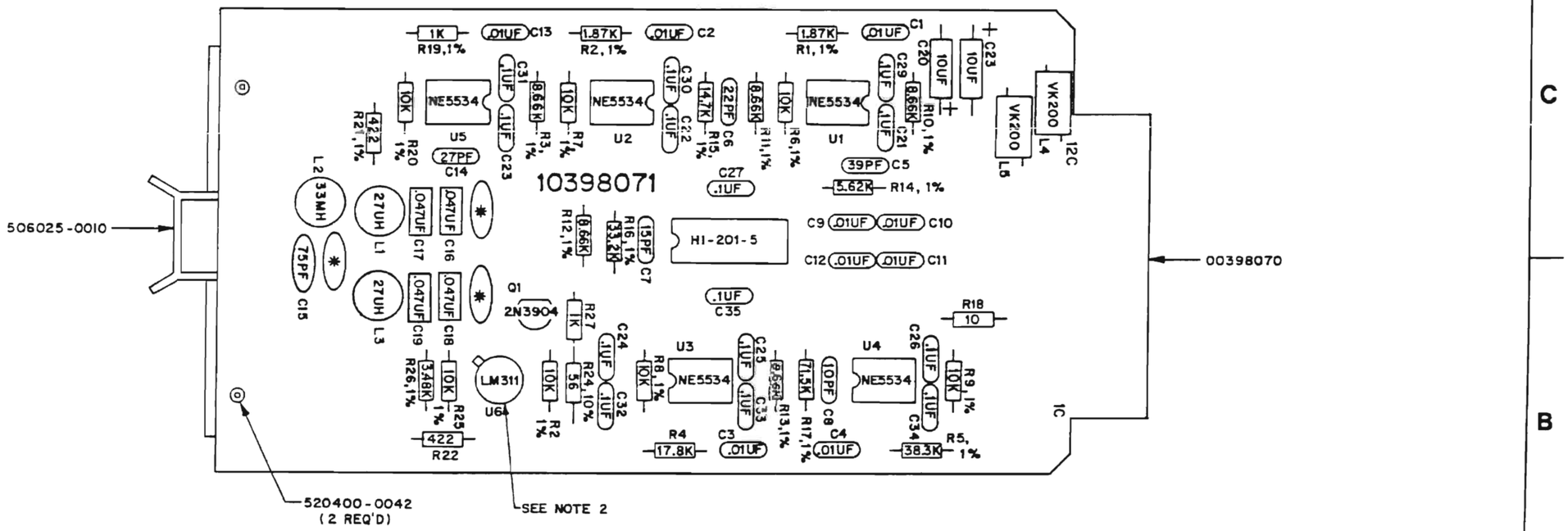
AUSTRON INC.
AUSTIN, TEXAS

SCHEMATIC, 2ND RF AMPLIFIER

SIZE 4 | CODE IDENT NO 24672 | 12398072

SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	4-27-81	
	A	CHANGED COMP. OUTLINE OF Q1 PER ECO 3506	4-12-81	



2. FORM LEADS OF U6 AND INSTALL WITH TAB POINTING TO PIN 8.
1. * = INDICATES SELECTED COMPONENTS.

NOTES:

NEXT ASSY	USED ON	REF DES	FIG NO
25498042	2100	1A1A2A2	5-4
25498281	2100F	1A1A2A2	5-4

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR
CHECKED
DRAWN LDP 3-13-81

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, 2ND RF AMPLIFIER

SIZE 3 | CODE IDENT NO 24672 | 10398071 | A

SCALE N/A | SHEET 1 OF 1

REVISIONS			
ZONE/LTR	DESCRIPTION	DATE	APPD

TRACK / HOLD

MULTIPLEXER

SHIFT REGISTER

BUFFER

A/D CONVERTER

CONTROL

OSCILLOSCOPE BUFFER

XA2 3F — P1 1C — RF IN

XA5 U — 4C — CYCLE HOLD

XA5 18 — 3F — PHASE HOLD

XA5 F — 11F — WINDOW

XA5 E — 3C — AMP HOLD

XA4 14 — 4F — LOW BYTE

XA4 R — 5C — HIGH BYTE

XA5 12 — 5F — STEP

C4 1000PF

C5 1000PF

C6 1000PF

U1-A, U1-B, U1-D — SN74LS08

U12, U13, U6 — HA2425 (IN, OUT, CON, V+ +12V, V- -12V)

U2-C, U2-B, U2-A, U2-D — HI-201-5

R1 27K

C1 1000PF

U3 — SN74LS221

U4-A, U4-B — SN74LS00

SN74LS175 U5

U10, U11 — SN74LS374

SN74LS00 U4-C 9,10

R2 1.5K

C3 1000 PF

U3 — SN74LS221

U9 — ADC 80Z (STAT, CONVERT, BIPOLAR OFFSET, COMP IN, ANALOG IN, +5 SUPPLY, DIG GND, ANAL GND, +12V DC SUPPLY, -12V DC SUPPLY; MSB 1 … LSB 12)

R3 8.2K

R4 27K

C2 .0033 UF

R6 8.2K

R7 8.2K

R9 8.2K

U7, U8 — NE5534

R5 100Ω

R8 100Ω

C7 2.2 PF

P1 10C +5V — +5VDC; C8 .1UF — GND

P1 10F DIGITAL GND

P1 12C +12VDC — L1 VK200 — +12VDC; C9 4.7 UF; C13 .1UF

P1 1F, 2C ANALOG GND — C10 .1UF; C14 .1UF; C11 4.7UF; C12 .1UF — ANALOG GND

P1 11C -12VDC — L2 VK200 — -12VDC

A/D IRQ — P1 12F — XA6 W

07 — 8C — J

06 — 9C — L

05 — 7C — 30

04 — 9F — 32

03 — 6C — H

02 — 8F — K

01 — 6F — 29

00 — 7F — 31

SCOPE VERT. — P1 2F — J8 REAR PANEL BNC (SCOPE VERTICAL)

NOTES:

1 UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4 WATT, 10%.

10398075	2100	1A1A2A3	5-5
10398075	2100F	1A1A2A3	5-5
NEXT ASSY	USED ON	REF DES	FIG NO

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED — DECIMALS ; FRACTIONS ; ANGLES

MATERIAL

ENGR

CHECKED 4-27-81

DRAWN ANE 11-18-80

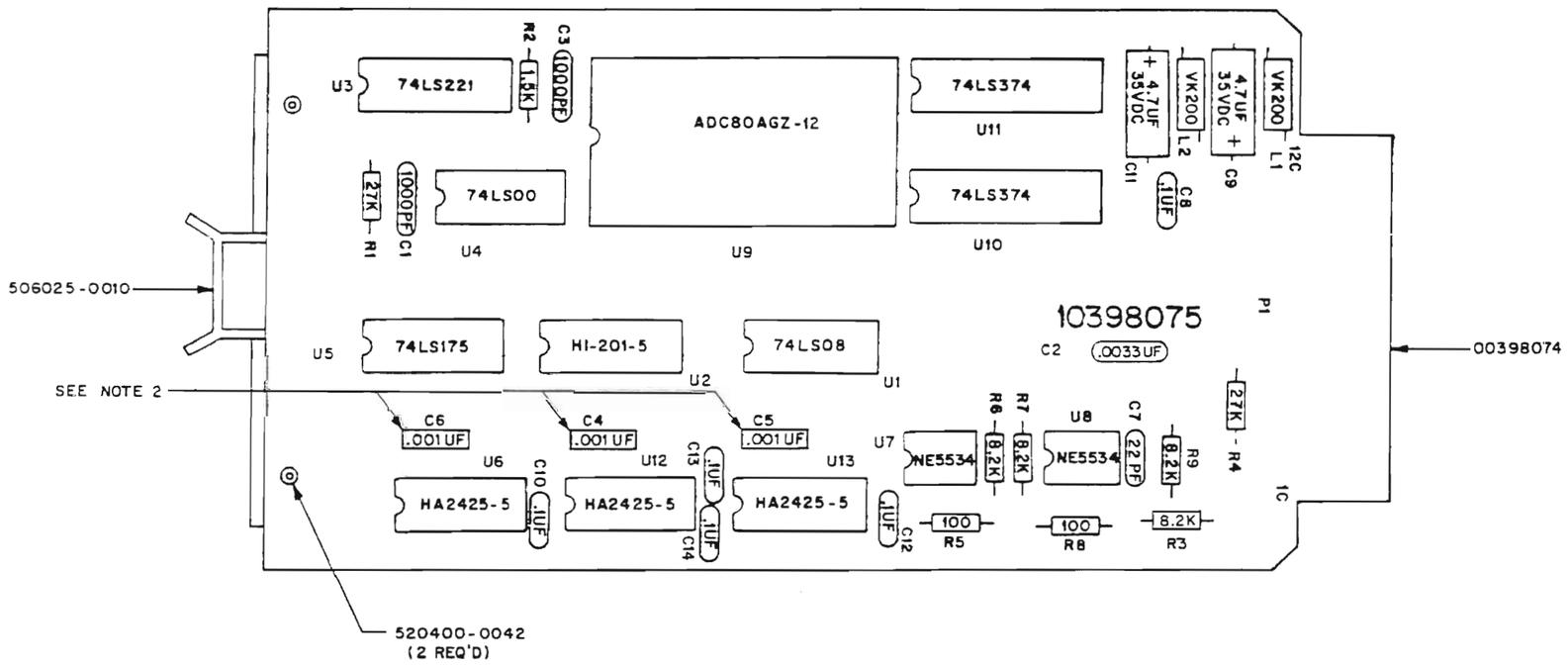
AUSTRON INC. AUSTIN, TEXAS

SCHEMATIC, ADC / SAMPLE HOLD

SIZE 4 | CODE IDENT NO 24672 | 12398076

SCALE N/A | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	4-23-81	RCP



2. C4, C5, & C6 MAY BE MARKED AS 1 NF, (SAME AS .001UF) AUSTRON PN 610008-0102.
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4 W, 10%.

NOTES:

NEXT ASSY	USED ON	REF DES	FIG NO
25438042	2100	1A1A2A2	5-6
25498281	2100F	1A1A2A3	5-6
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL

ENGR
CHECKED
DRAWN LDP 11-26-80

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, ADC/ SAMPLE HOLD

SIZE	CAGE IDENT NO	
3	24672	10398075

SCALE N/A SHEET 1 OF 4

IPPS MASK REGISTER

RF GAIN CONTROL REGISTER

IPPS PHASE SHIFTER

DOUBLER A

10MHZ PHASE LOCKED LOOP

DOUBLER B

MAIN PHASE SHIFTER

AUXILIARY PHASE SHIFTER

DIVIDER

TOC DETECTOR

IPPS DIVIDER

AUXILIARY PHASE SHIFTER CONTROL A

AUXILIARY PHASE SHIFTER CONTROL B

REGISTER SELECTOR

TOC SYNCHRONIZER

IPPS SYNCHRONIZER

IPPS OUTPUT

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 W, 10%, WITH VALUES IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROFARADS

ZONE	LTR	DESCRIPTION	DATE	APPD
		REVISIONS		
	—	RELEASED	10-5-81	KDE

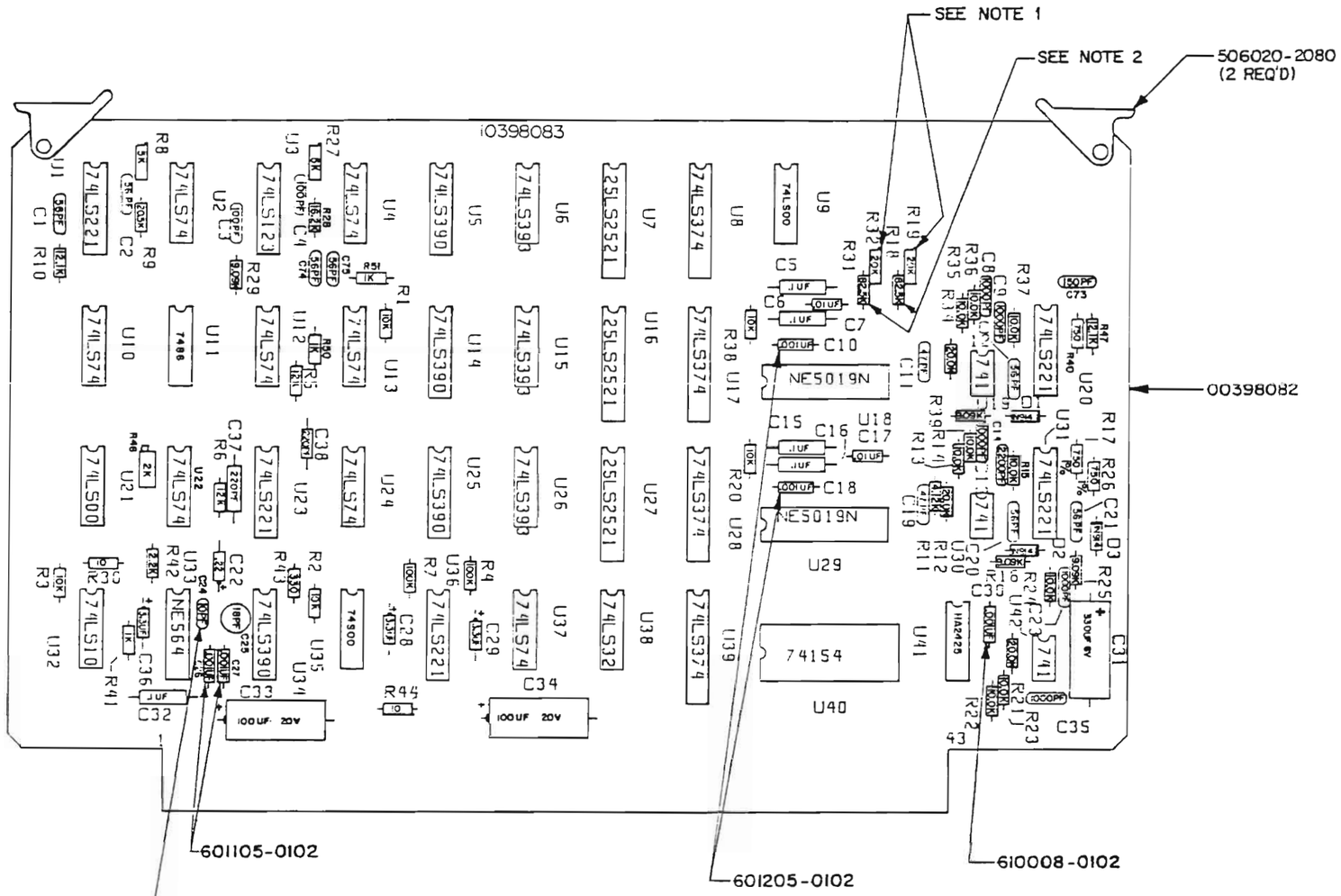
10398083	2100	AAA2A4	5-7
NEXT ASSY	USED ON	REFDES	FIG NO
APPLICATION			
ENGR	J. Darnell	11/3/81	
CHECK	R. Simmons	10/5/81	
DRFTSMN	SCHMIDT	1-28-80	

AUSTRON INC.
AUSTIN, TEXAS

SCHEMATIC,
1 MHZ PHASE SHIFTER

4	24672	123 98084
SCALE NONE		SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	7-9-81	RDB



2. THESE COMPONENTS MAY BE MOUNTED ON BACK SIDE OF BOARD IF CLEARANCE IS NEEDED.

1. INSTALL R19 & R32 BEFORE R18 & R31 ARE INSTALLED TO INSURE PROPER MOUNTING.

NOTES:

25498042	2100	IA1A2A4	5-8
NEXT ASSY	USED ON	REF DES	FIG NO

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR		6/2/81
CHECKED		7/9/81
DRAWN	larry phillips	5/8/81

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, 1MHZ PHASE SHIFTER

SIZE	CODE IDENT NO	
3	24672	10398083

SCALE N/A SHEET 1 OF 1

REVISIONS

LTR	DESCRIPTION	DATE	APPD

P1

D7 D6 D5 D4 D3 D2 D1 D0 Q

A0 A1 A2 A3 A8 DNSØC

IPPS OUT

TOC IRQ

SW2 IRQ

SW1 IRQ

1PPS IRQ

A/D IRQ

1MHZ(A)

REGISTER SELECTOR

SN74154 U48

U18 SN74LS32

D/A CONVERTER

U28 NE5019N DATA COMP

C9 .01UF C8 .1UF R11 10K 1% +12V R12 1.5K 1%

C7 .001UF C6 150PF C5 .1UF

C12 .1UF R13 2K 1% C13 .01UF

U32 SN74LS374 U31 SN74LS374

U43 DAC80Z CB1-V

C14 1UF C11 .1UF C10 .01UF

SCAN STROBE OUTPUT

10 µSEC 8 COMP

SCAN STROBE

IRQ REGISTER

U14A U14B 74LS74

R1, 4.7K R2, 4.7K R3, 4.7K R4, 4.7K R5, 4.7K R6, 4.7K R7, 4.7K R8, 4.7K

U1A SN74LS32

U30 SN74LS240

U17B U15A U17A U15B U16B U16A 74C74

U29 SN74LS240

U27 SN74LS374

RECEIVER MASK

U2 SN74LS30

U10A SN74LS10

U3 SN74LS74

MASK MATCH REGISTER A

MASK MATCH REGISTER B

U36 U35 U34 U33 U37 SN74LS374

U4C SN74LS86

MASK MATCH COMPARATOR

U3A SN74LS74

U46 U45 25LS2521

U24 74393

U47 U44 74393

MASK MATCH DIVIDER

U18A U18B 7474

MASK MATCH OUTPUT / MASK MATCH STROBE

P2

IRQ

CONTINUED ON SHEET 2

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4W, 10%, WITH VALUES IN OHMS

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS ± FRACTIONS ± ANGLES
MATERIAL

AUSTRON INC
AUSTIN, TEXAS

SCHEMATIC,
ACQUIRE/TRACK

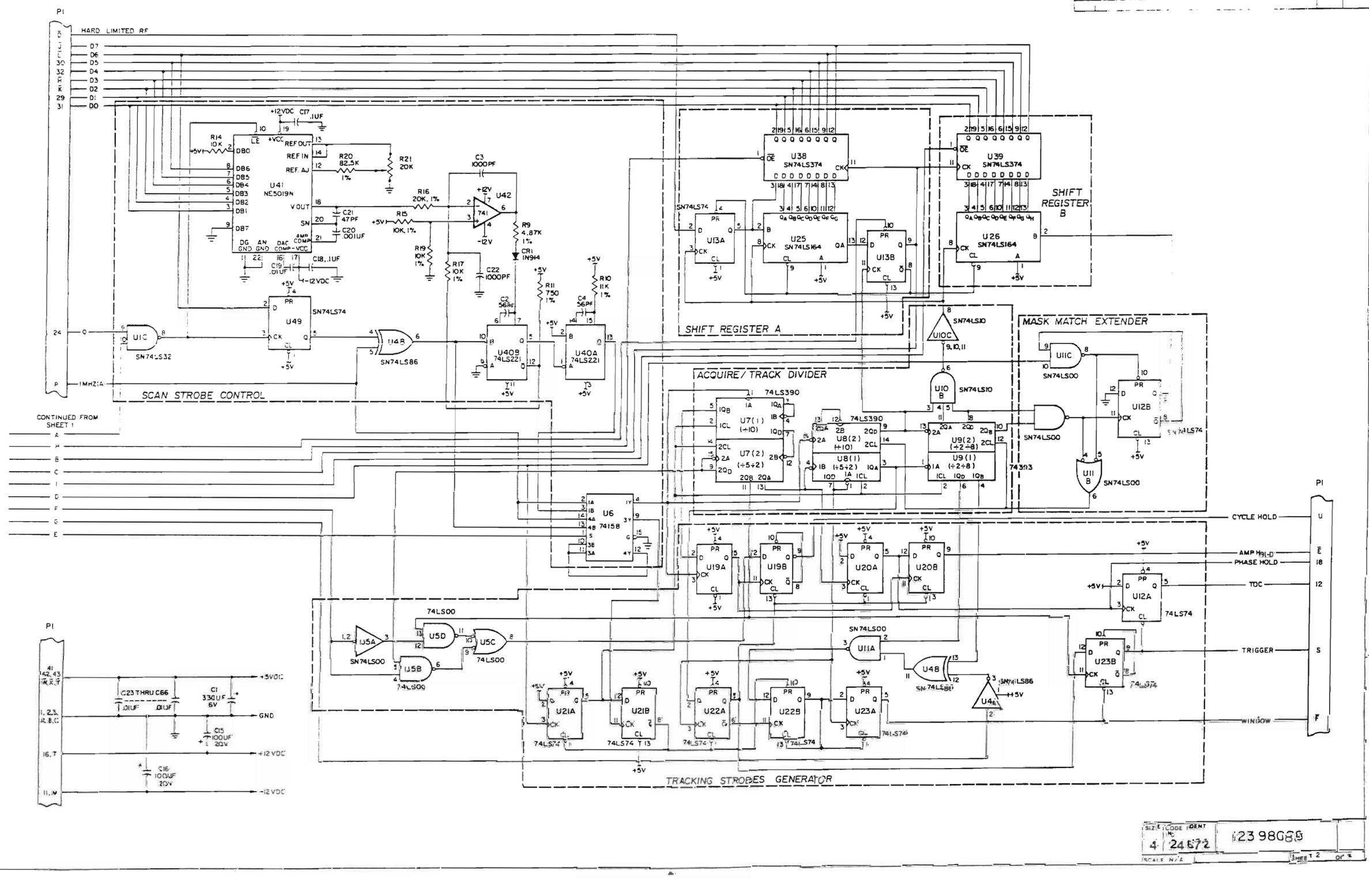
103 98087	2100	1A1A2A5	5-9
NEXT ASSY	USED ON	REF DES	FIG NO

APPLICATION

DRAWN SCHMIDT 12 IT BOYSAK NA

SIZE 4 | FSCM NO. 24672 | DWG NO. 123 98088

SHEET 1 OF 2


P1
HARD LIMITED RF
D7
D6
D5
D4
D3
D2
D1
D0
+12VDC
C17 .1UF
R14 10K
+5V
LE
+VCC
REFOUT
REFIN
REF. ADJ
R20 82.5K 1%
R21 20K
U41 NE5019N
DB0
DB6
DB5
DB4
DB3
DB2
DB1
DB7
VOUT
SN
AMP COMP
DG GND
AN GND
DAC COMP
-VCC
C21 47PF
C20 .001UF
C18, .1UF
C19 .01UF
-12VDC
C3 1000PF
R16 20K, 1%
R15 10K, 1%
R19 10K 1%
R17 10K 1%
C22 1000PF
U42 741
+12V
-12V
R9 4.87K 1%
CR1 IN914
R11 750 1%
R10 11K 1%
C2 56PF
C4 56PF
U49 SN74LS74
U1C SN74LS32
U14B SN74LS86
U40B 74LS221
U40A 74LS221
SCAN STROBE CONTROL
24
P
1MHZ/A
CONTINUED FROM SHEET 1
A
H
B
C
I
D
F
G
E
SHIFT REGISTER A
U38 SN74LS374
U39 SN74LS374
SHIFT REGISTER B
U13A SN74LS74
U25 SN74LS164
U13B
U26 SN74LS164
ACQUIRE/TRACK DIVIDER
74LS390
U7(1) (÷10)
U7(2) (÷5÷2)
U8(2) (÷10)
U8(1) (÷5÷2)
U9(2) (÷2÷8)
U9(1) (÷2÷8)
74393
U6 74158
U10C SN74LS10
U10B SN74LS10
9,10,11
MASK MATCH EXTENDER
U11C SN74LS00
U12B SN74LS74
U11B SN74LS00
U19A
U19B
U20A
U20B
U12A 74LS74
U11A SN74LS00
U23B 74LS74
U5A SN74LS00
U5B 74LS00
U5D
U5C 74LS00
U21A 74LS74
U21B 74LS74
U22A 74LS74
U22B 74LS74
U23A 74LS74
U4B SN74LS86
U4A SN74LS86
TRACKING STROBES GENERATOR
CYCLE HOLD
AMP HOLD
PHASE HOLD
TOC
TRIGGER
WINDOW
P1
41 42, 43 W, X, Y
1, 2, 3 A, B, C
16, T
11, N
C23 THRU C66 .01UF
C1 330UF 6V
C15 100UF 20V
C16 100UF 20V
+5VDC
GND
+12 VDC
-12 VDC
SIZE 4
CODE IDENT NO 24672
123 9808 9
SCALE N/Z
SHEET 2 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	1	RELEASE	7-9-81	
	1A	U9, 24 WERE 74LS393; U18 WAS 74LS74. ECO 3914	9-24-81	

506020-2080
(2 PLACES)

00398086

601205-0102

10398087

25498042	2100	1A1A2A5	5-10
NEXT ASSY	USED ON	REF DES	SIG NO

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR		6/2/81
CHECKED		7/9/81
DRAWN	LDP	15-JUL-81

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, ACQUIRE / TRACK

SIZE	CODE IDENT NO.		
3	24672	10398087	A

SCALE N/A SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	–	RELEASED	10-5-81	

REGISTER SELECT

CARRIER RELAY

FRONT PANEL INTERFACE

REGISTER

INTERFACE A

INTERFACE B

INTERFACE C

MPU

RAM

EPROM

QUADRATURE CLOCK

EXT / REF BUFFER

RAM / EPROM ADDRESS DECODER

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W, 10%, WITH VALUES IN OHMS.

TOLERANCES		
UNLESS OTHERWISE SPECIFIED		
DECIMALS	FRACTIONS	ANGLES
MATERIAL		

AUSTRON INC.
AUSTIN, TEXAS

SCHEMATIC, MPU/MEMORY

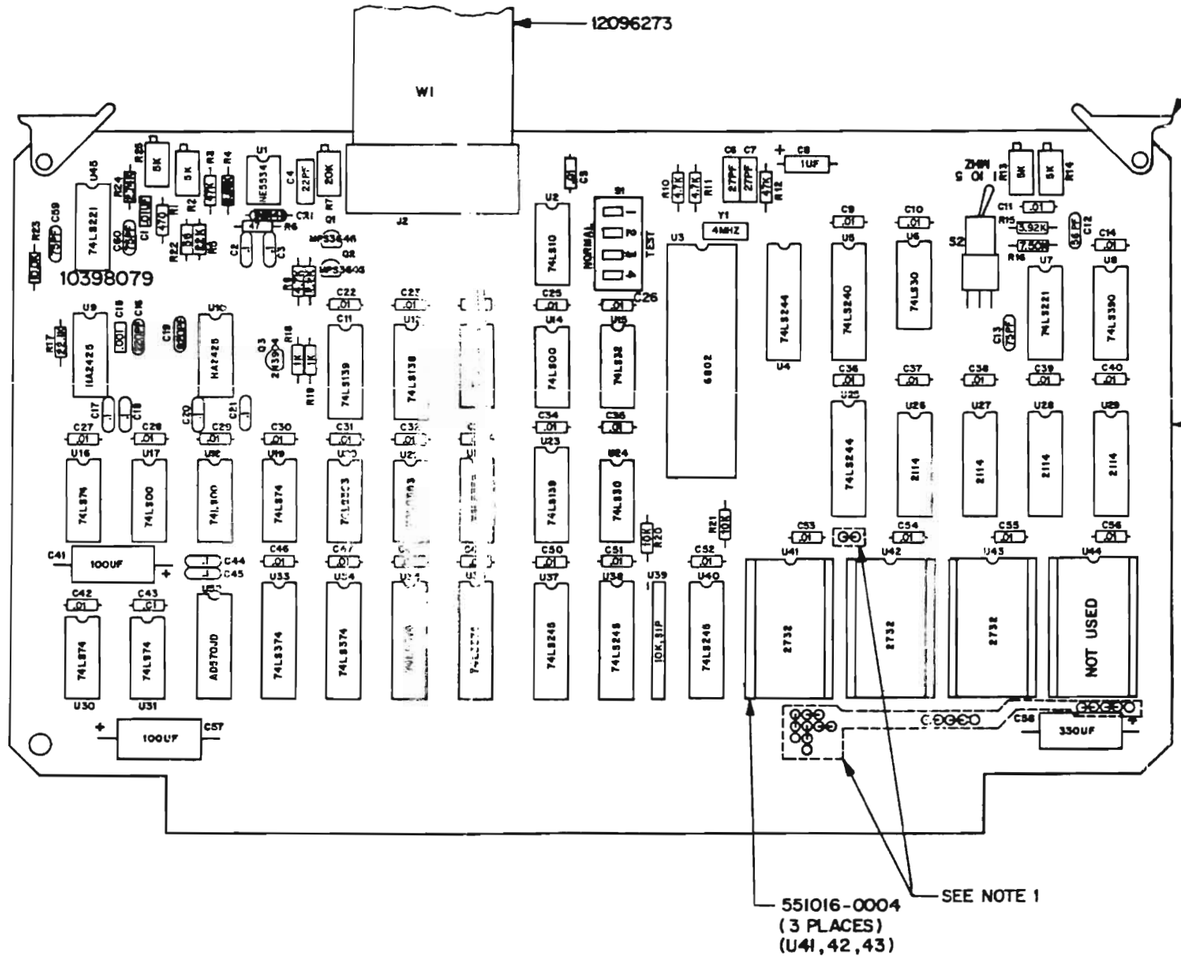
10398079	2100	1A1A2A6	5-11
NEXT ASSY	USED ON	REF DES	FIG NO
APPLICATION			

ENGR			
CHECKED			
DRAWN	LDP	2-13-81	

SIZE 4 | CODE IDENT NO. 24672 | 12398080

SCALE | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	7-9-81	RDB
	A	REVISED PARTS LIST PER ECO. 3912	9-23-81	RDB
	B	ADDED REF DES W1 & C26 PER ECO 3930	11-2-81	RDB



1. INSTALL JUMPERS USING AWG 22 BUS WIRE. USE TEFLON INSULATION WHERE REQUIRED.

NOTES:

25498042	2100	1A1A2A6	5-12
NEXT ASSY	USED ON	REF DES	FIG NO
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED

DECIMALS	FRACTIONS	ANGLES

MATERIAL:

ENGR	J.J. Powell	6/24/81
CHECKED	R. Barker	7-9-81
DRAWN	larry phillop	5-8-81

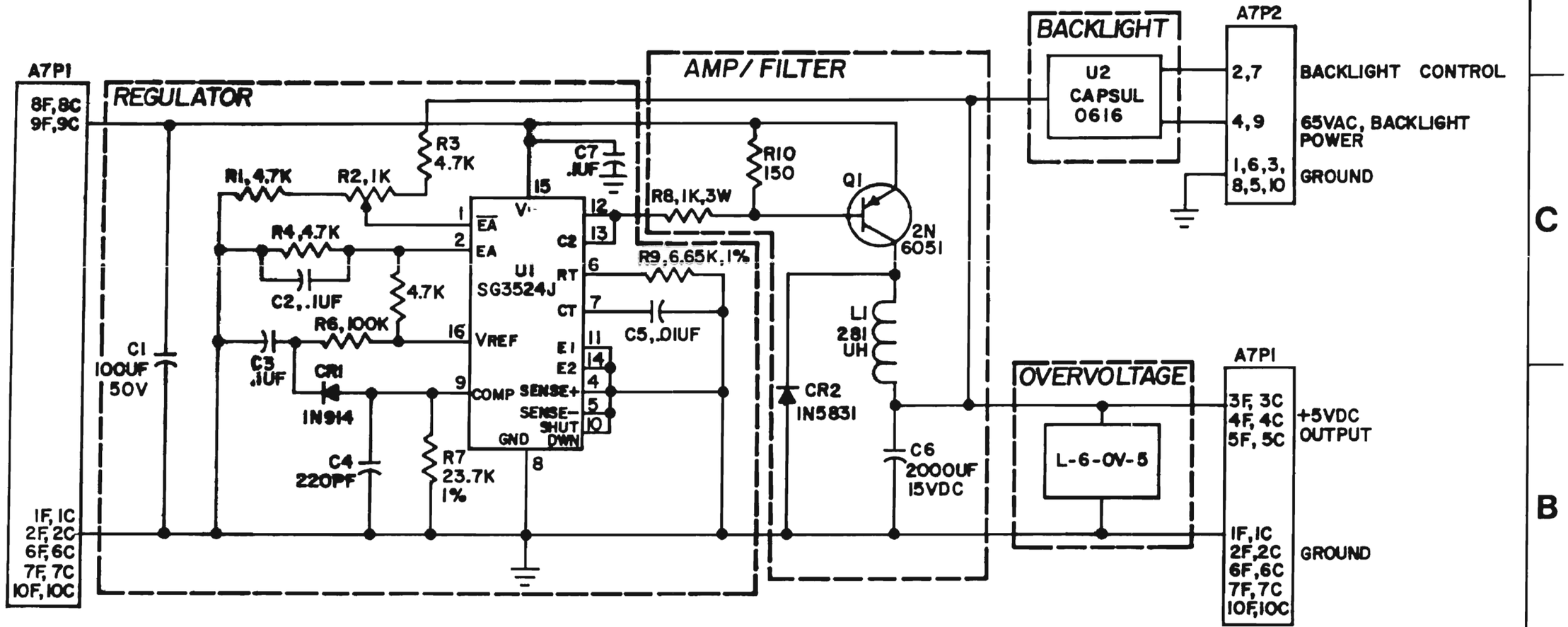
AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, MPU / MEMORY

SIZE	CODE IDENT NO.		
3	24672	10398079	B

SCALE N/A SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	4-10-81	ROB



NOTES:

1. ALL RESISTORS ARE 1/4W, 10% UNLESS OTHERWISE SPECIFIED.

25498042	2100	1A1A2A7	5-13
25498281	2100F	1A1A2A7	5-13
NEXT ASSY	USED ON	REF DES	FIG NO
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED

DEC	FRAC	ANG

MATERIAL:

ENGR		
CHECK	A. Becker	4-10-81
DRFTMN	LDP	4-2-81

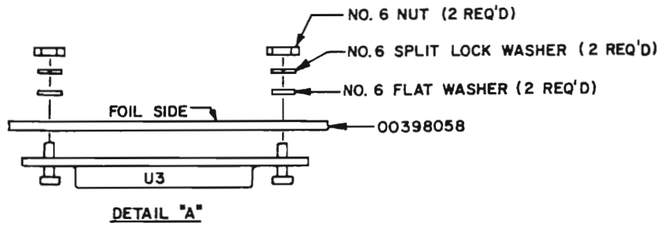
AUSTRON INC
AUSTIN, TEXAS

SCHEMATIC,
+5V SWITCH REGULATOR

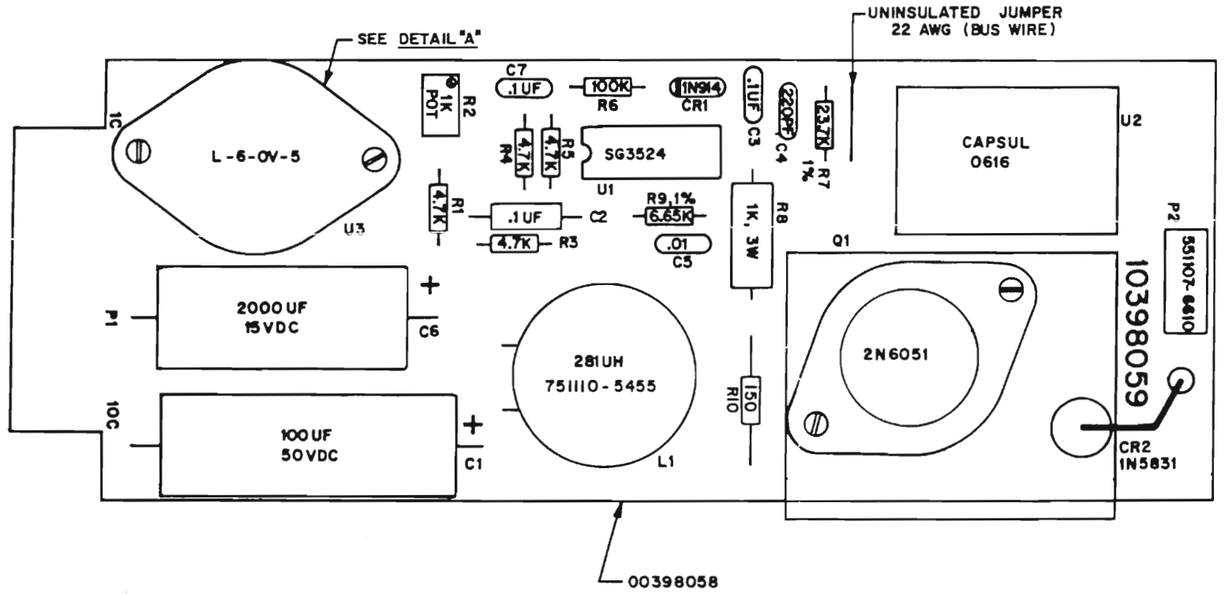
SIZE	CODE IDENT NO	
2	24672	12398060

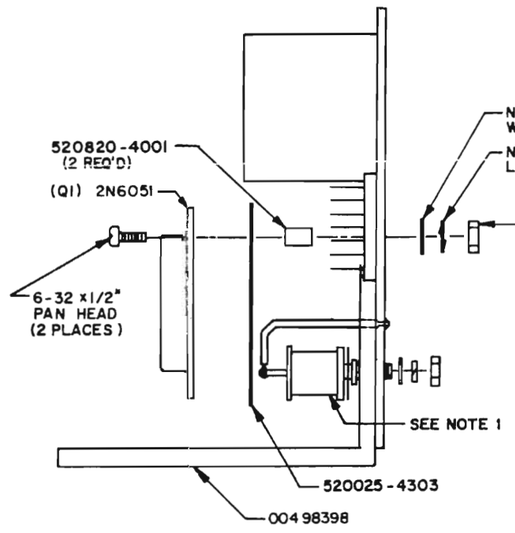
SCALE N/A | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	4-10-84	RDB



DETAIL "A"





NOTES:
1. USE STANDARD MOUNTING HARDWARE FOR CR2.

NEXT ASSY	USED ON	REF DES	FIG NO
25498042	2100	1A1A2A7	5-14
25498281	2100F	1A1A2A7	5-14
APPLICATION			

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR		
CHECKED	R. Barker	4-10-84
DRAWN	LDP	11-26-80

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, +5 VOLT REGULATOR

SIZE	CODE IDENT NO.	
3	24672	10398059

SCALE N/A SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	–	RELEASED	10-5-81	RJB

NUMERIC DISPLAY

DS2

8 DIGIT LCD

ICM7211AMIPL U8

ICM7211AMIPL U7

1A1A2A6 P2 J1

READ SWITCHES

STATUS LOW

STATUS HIGH

READ LOW

READ HIGH

BUFFER

74LS244 U5

SWITCH ENCODERS

MM74C923 (IC-A) U6

MM74C923 (IC-B) U4

SWITCHES

LATCH / INDICATORS

74LS374 U3

74LS374 U2

BACKLIGHT

ENUNCIATOR DRIVERS

LC DISPLAY BACKLIGHT DS1

65VAC

BACKLIGHT CONTROL

1A1A2A7 P1 J1

SWITCH HIGH

SWITCH LOW

1A1A2A6 J1 P2

2. ▨ = THESE PARTS NOT USED WITH MODEL 2100F

1. ALL RESISTORS ARE 470 OHMS 1/8W, 10% UNLESS OTHERWISE SPECIFIED.

NOTES:

10398063	2100F	1A1A1	5-15
10398598	2100	1A1A1	5-15
NEXT ASSY	USED ON	REF DES	FIG NO

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMALS | FRACTIONS | ANGLES

MATERIAL

ENGR			10/31/81
CHECKED			10/5/81
DRAWN	LDP	12-31-80	

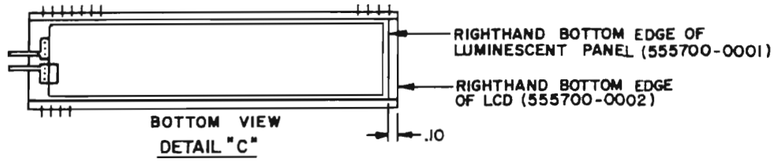
AUSTRON INC. AUSTIN, TEXAS

SCHEMATIC, FRONT PANEL LCD DISPLAY / KEYBOARD

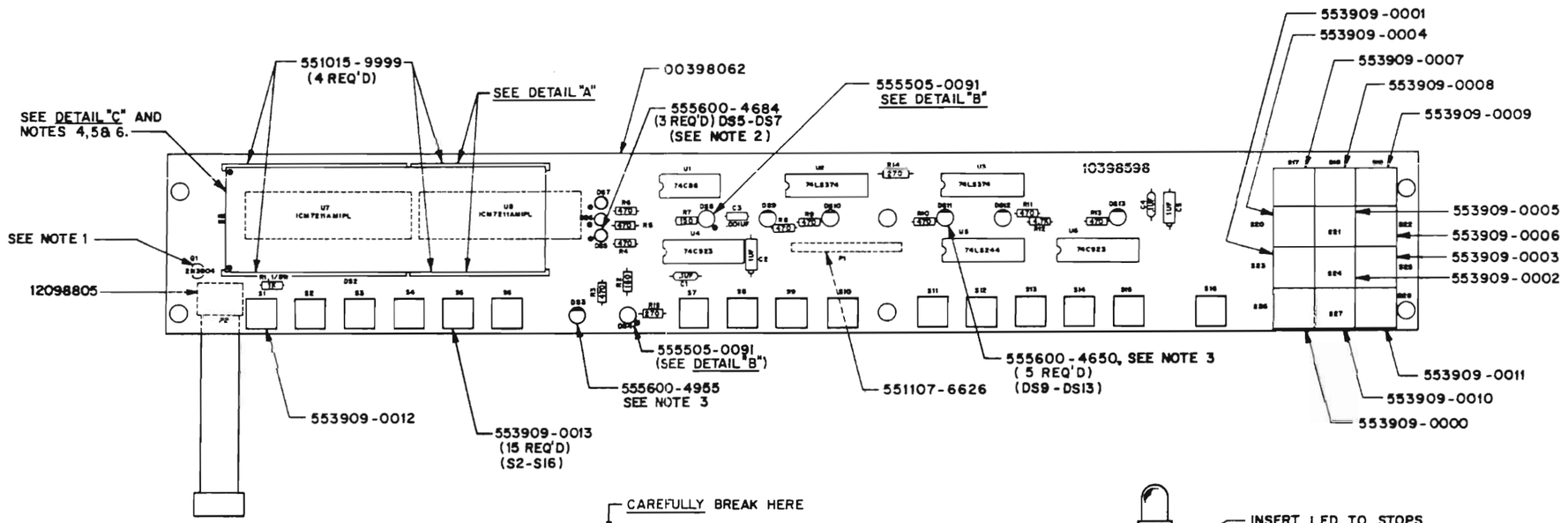
SIZE 4 | CODE IDENT NO. 24672 | 12398064

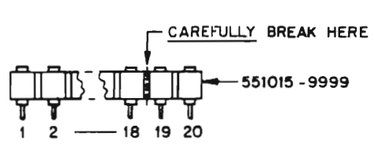
SCALE N/A | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	–	RELEASED	5-8-81	

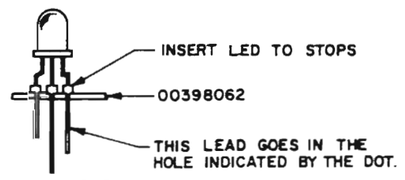


BOTTOM VIEW
DETAIL "C"





DETAIL "A"



DETAIL "B"

7. MOUNT ALL SWITCHES FLAT ON THE PCB.
6. A RECOMMENDED ASSEMBLY PROCEDURE FOR THE LCD AND BACKLIGHT COMBINATION, IS TO INSTALL THE SOCKET STRIPS ON THE LCD PINS FIRST, THEN INSERT INTO THE PCB, AND HAND SOLDER.
5. ASSEMBLE LC DISPLAY TO LUMINESCENT PANEL AS SHOWN IN DETAIL "C."
4. LOOKING AT THE TOP SURFACE OF THE LCD, THE LEFT HAND SIDE IS IDENTIFIED BY 2 SMALL DOTS.
3. INSTALL THESE LEDS SO THAT THEY EXTEND PAST THE SURFACE OF THE FRONT PANEL THE SAME AMOUNT AS 555505-0091.
2. THESE 3 LEDS SHOULD COME JUST TO THE SURFACE OF THE FRONT PANEL. THE LONG LEAD GOES IN THE HOLE INDICATED BY THE DOT.
1. TOP OF TRANSISTOR MUST NOT EXTEND ABOVE TOP OF LC DISPLAY.

NOTES:

NEXT ASSY	USED ON	REF DES	FIG NO
	2100		5-16

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL: N/A

ENGR		
CHECKED	R Barker	5-8-81
DRAWN	LDP	1/14/81

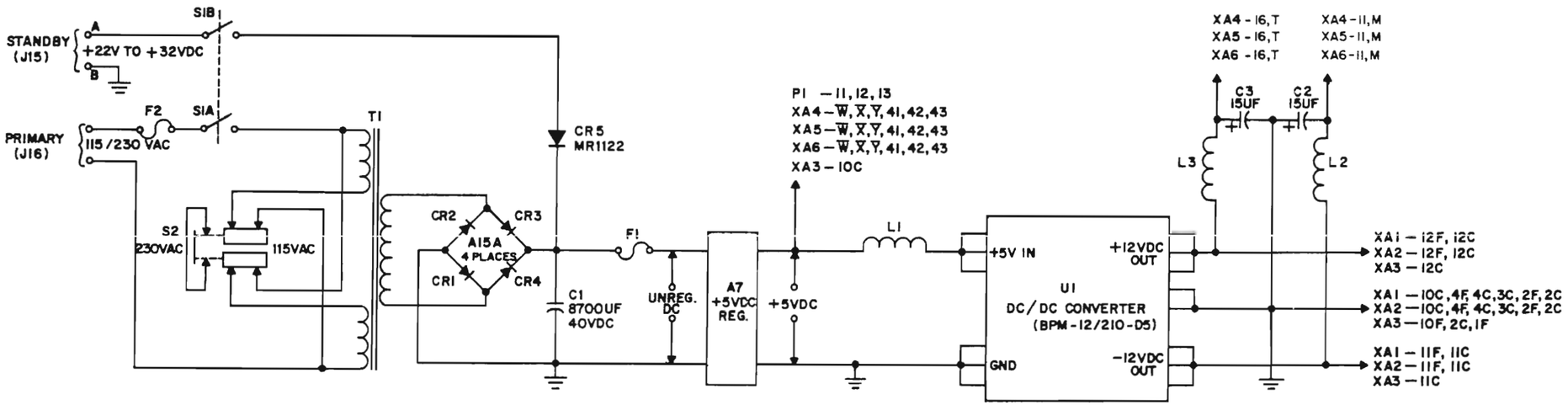
AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, FRONT PANEL LCD DISPLAY / KEYBOARD

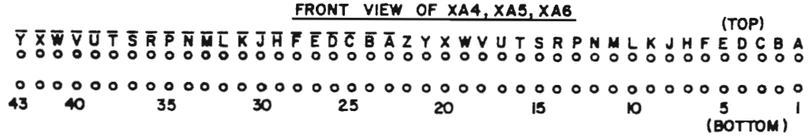
SIZE	CODE IDENT NO	
3	24672	10398598

SCALE 1/1 SHEET OF

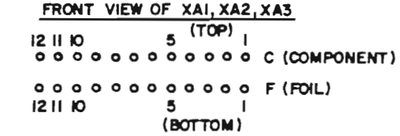
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	6-2-81	
	A	REVISED PER ECO # 3866	8-17-81	



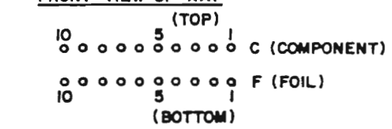
FRONT VIEW OF XA4, XA5, XA6



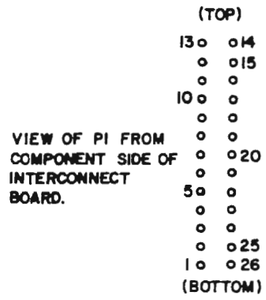
FRONT VIEW OF XA1, XA2, XA3



FRONT VIEW OF XA7



VIEW OF P1 FROM COMPONENT SIDE OF INTERCONNECT BOARD.



10398026	2100	1A1	5-17
10398026	2100F	1A1	5-17
NEXT ASSY	USED ON	REF DES	FIG NO

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED

DECIMALS	FRACTIONS	ANGLES

MATERIAL:

ENGR		
CHECKED		6-2-81
DRAWN	LDP	4-23-81

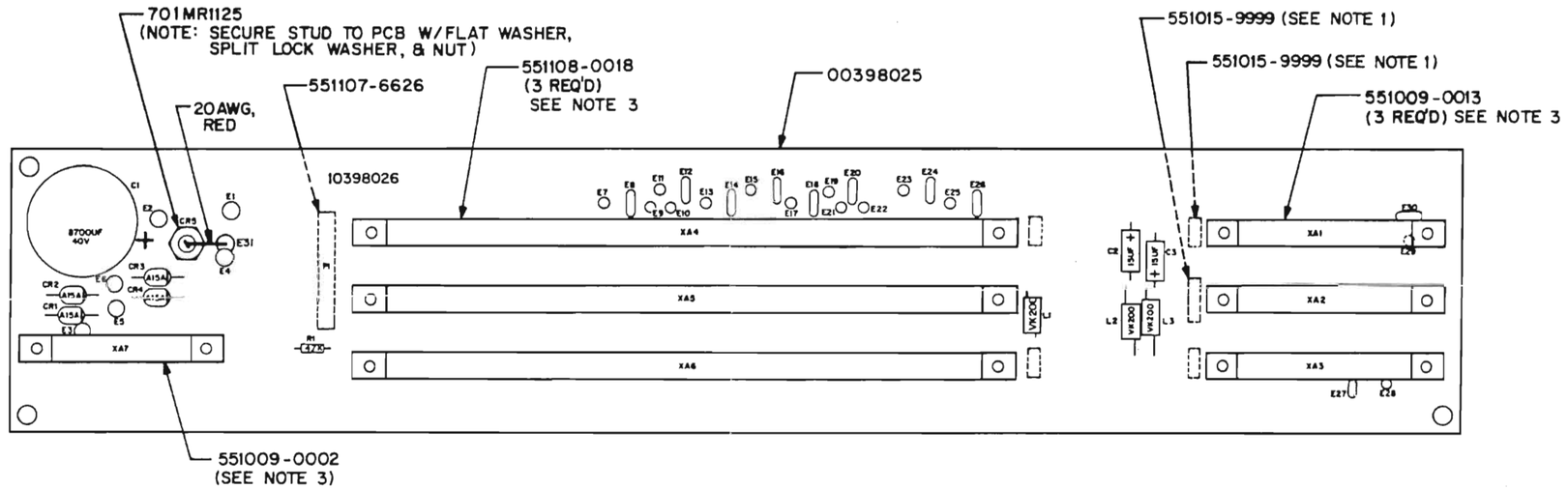
AUSTRON INC.
AUSTIN, TEXAS

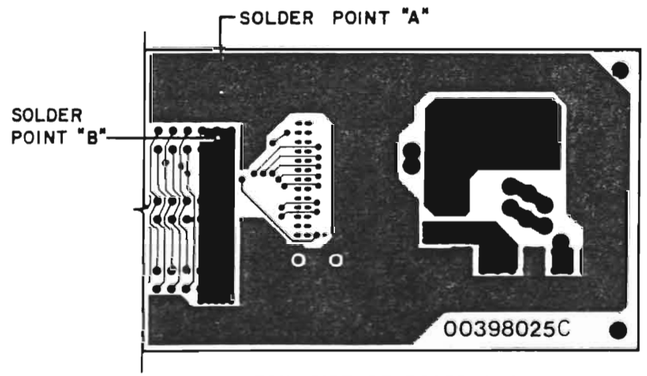
SCHEMATIC, POWER DISTRIBUTION AND INTER-CONNECT PIN OUTS

SIZE	CODE IDENT NO.		
3	24672	12398766	A

SCALE | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	4-14-81	RDB
	A	CHANGED NOTE 2 PER ECO 3804	6-11-81	RDB
	B	DELETED NOTE 2 & REVISED NOTE 1, PER ECO. 3836	8-7-81	RDB
	C	ADDED VIEW OF FOIL SIDE, PER ECO. 3984	12-16-81	RDB





FOIL SIDE OF BOARD SHOWN

3. INSTALL ALL CONNECTORS CLOSE TO THE BOARD WITH NO TILT.
2. DELETED

1. BREAK SOCKET STRIP TO FORM 4 SECTIONS WITH 3 PINS, AND ONE SECTION WITH 4 PINS. REMOVE 2 MIDDLE PINS FROM THE 4 PIN SECTION.

NOTES:

NEXT ASSY	USED ON	REF DES	FIG NO
11498599	2100	1A1A2	5-18
11498490	2100F	1A1A2	5-18
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR		4-14-81
CHECKED		4-14-81
DRAWN	LDP	3-5-81

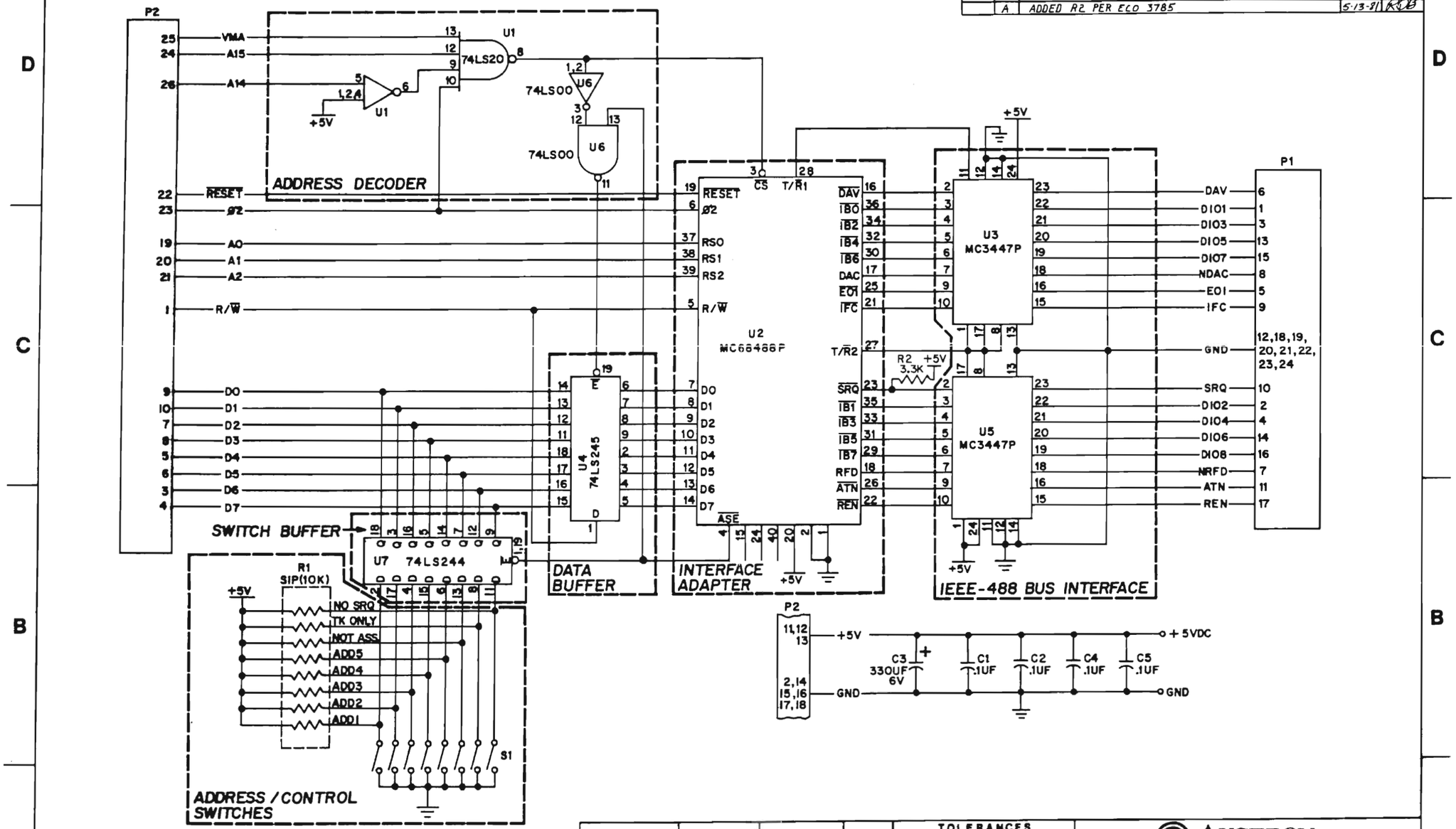
AUSTRON INC. AUSTIN, TEXAS

PCB ASSY, INTERCONNECT

SIZE	CODE IDENT NO		
3	24672	10398026	C

SCALE 1/1 SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	–	RELEASED	4-16-81	
	A	ADDED R2 PER ECO 3785	5-13-81	



12898484	2100F	1A1A3	5-19	
12898484	2100	1A1A3	5-19	
NEXT ASSY	USED ON	REF DES	FIG NO	
APPLICATION				

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR		4-16-81
CHECKED		4-16-81
DRAWN	LDP	12-2-80

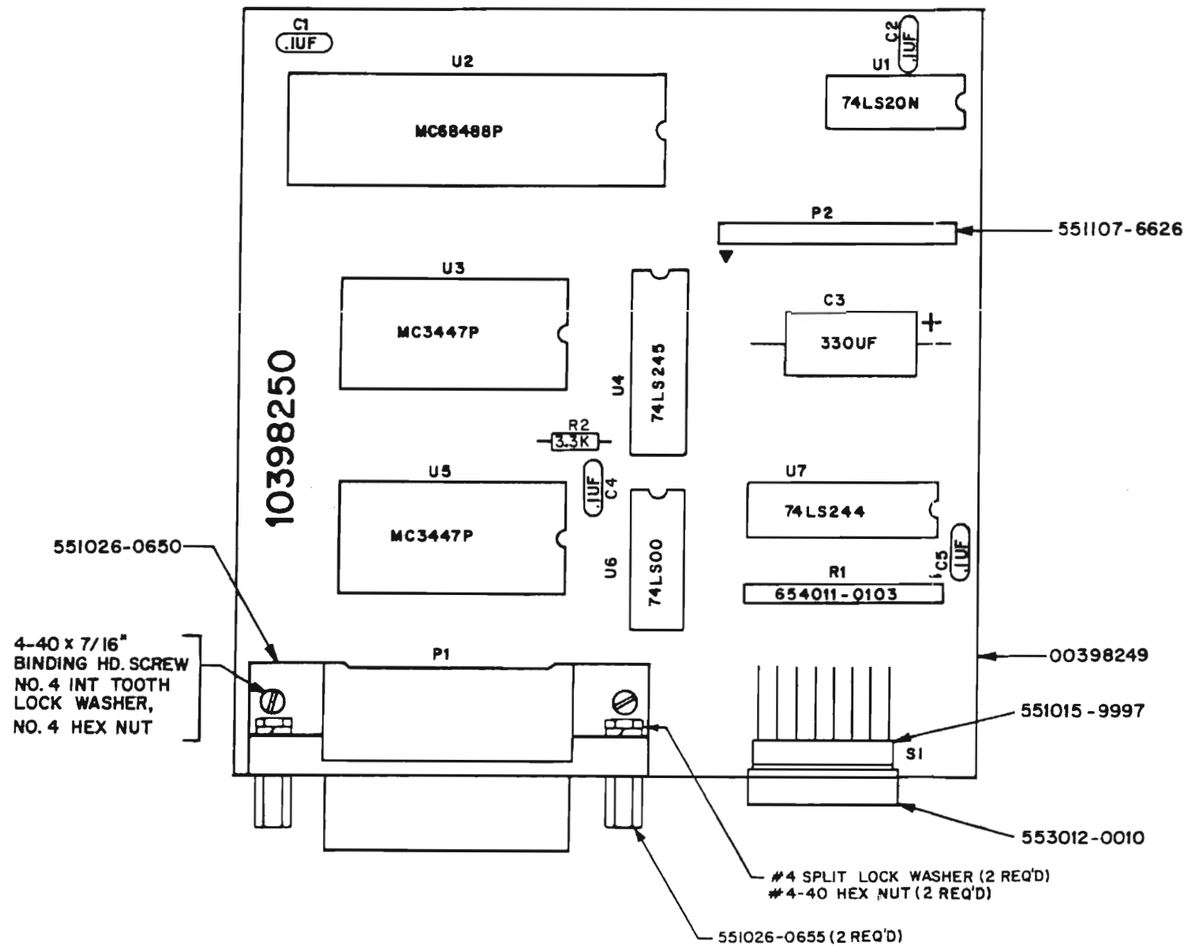
AUSTRON INC.
AUSTIN, TEXAS

SCHEMATIC, GENERAL PURPOSE INTERFACE BUS

SIZE	CODE IDENT NO.		
3	24672	12398251	A

SCALE N/A SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	–	RELEASED	4-16-81	RDB
	A	ADDED R2 & MTG HARDWARE TO P1 PER ECO 3785	5-13-81	RDB



NEXT ASSY	USED ON	REF DES	FIG NO
	2100		5-20
	2100F		5-20

APPLICATION

TOLERANCES (UNLESS OTHERWISE SPECIFIED)
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR
CHECKED
DR AWD LDP 12-4-80

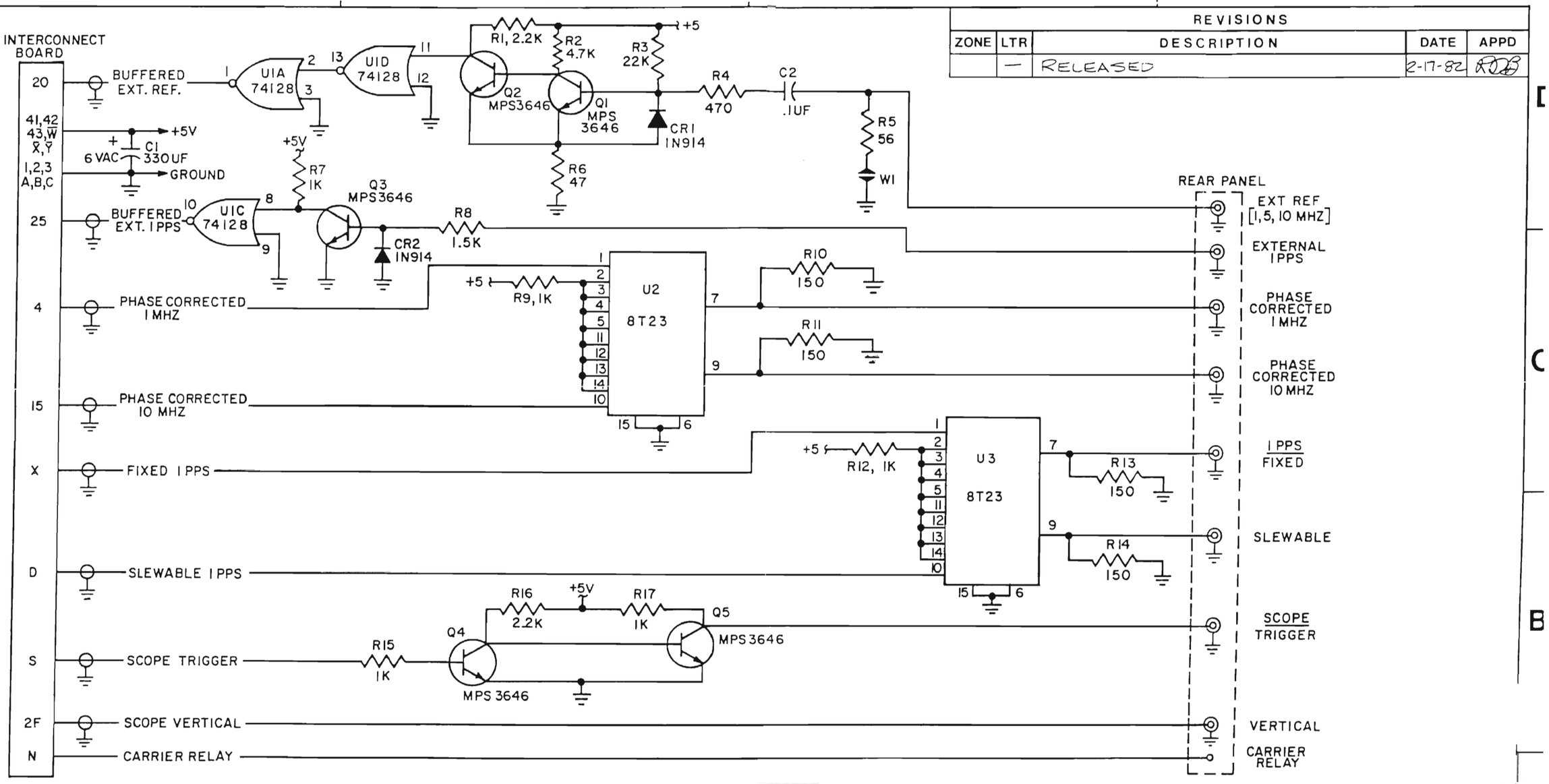
AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, GENERAL PURPOSE INTERFACE BUS

SIZE	CODE IDENT NO.		
3	24672	10398250	A

SCALE N/A SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	2-17-82	



10399019	2100F	1A1A4	5-21
10399019	2100	1A1A4	5-21
NEXT ASSY	USED ON	REF DES	FIG NO
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED

DEC	FRAC	ANG

MATERIAL:

ENGR	K. BOWELL	
CHECK		2-17-82
DRFTMN	SCHMIDT	2-15-82

AUSTRON INC
AUSTIN, TEXAS

SCHEMATIC, INPUT/OUTPUT BUFFERS

SIZE	CODE IDENT NO		
2	24672	12399020	
SCALE N/A		SHEET 1 OF 1	

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4W, 10%, WITH VALUES IN OHMS
   ALL CAPACITANCE VALUES ARE IN MICROFARADS

NOTES:

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	2-17-82	R.O.S

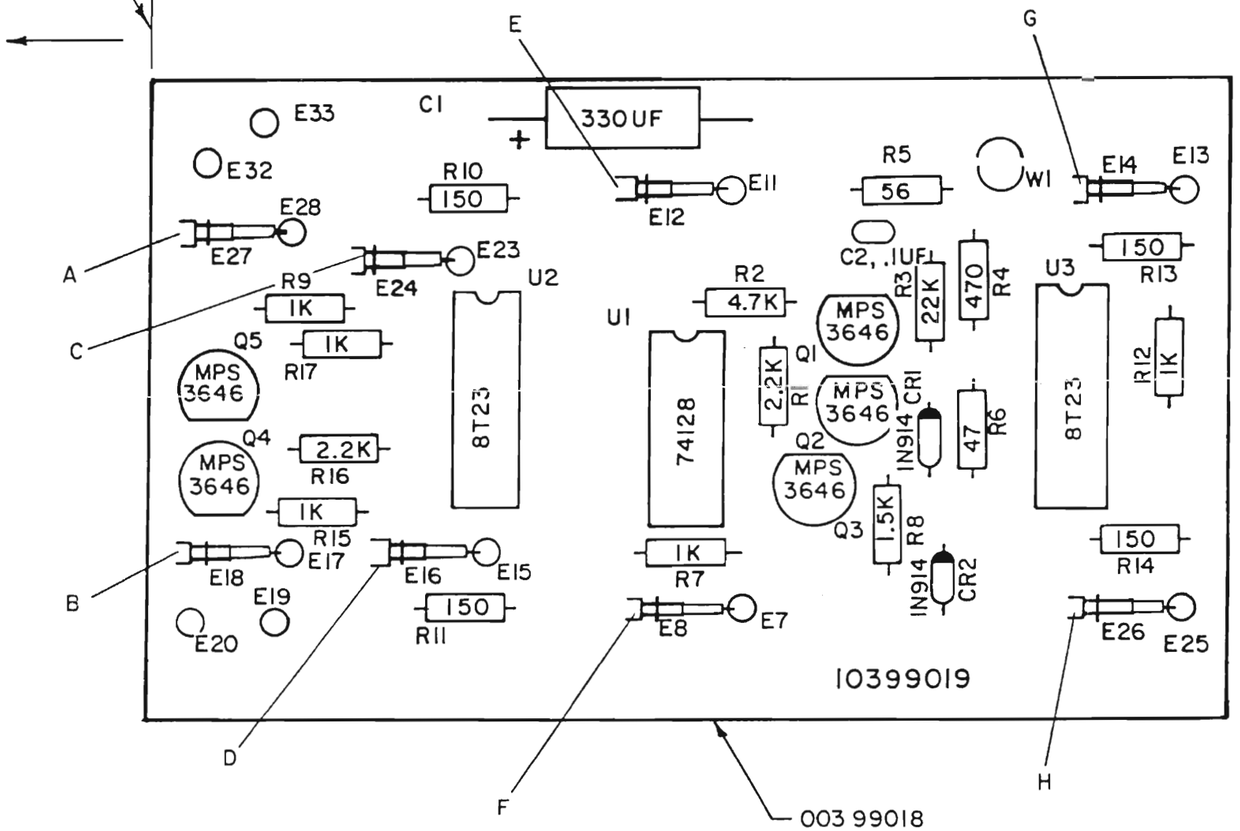


TABLE A

CABLE	LENGTH	CONNECTS TO
A	12.0"	A2 E27, E28
B	8.9"	A2 E17, E18
C	7.6"	A2 E23, E24
D	9.2"	A2 E15, E16
E	10.4"	A2 E11, E12
F	10.9"	A2 E7, E8
G	9.7"	A2 E13, E14
H	7.3"	A2 E25, E26
RED/BLK T. PR.	13.0"	A2 E32, E33
YEL/BLK T. PR.	8.9"	A2 E19, E20

3. THIS PCB MUST BE TESTED PRIOR TO INSTALLATION IN CHASSIS.
2. TO INSTALL COAX AND TWISTED PAIRS SOLDER ONE END TO BOARD THEN CUT TO LENGTH GIVEN IN TABLE A MEASURING FROM LEFT EDGE OF BOARD.
1. NO SERVICE LOOPS ON COAX CENTER CONDUCTORS

NOTES:

NEXT ASSY	USED ON	REF DES	FIG NO
10998404	2100F	1A1A4	5-22
10998047	2100	1A1A4	5-22

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED

DEC	FRAC	ANG

MATERIAL:

ENGR	J. R. HOWELL	
CHECK		
DRFTMN	SCHMIDT	2-10-82

AUSTRON INC
AUSTIN, TEXAS

P.C.B. ASSY, INPUT/OUT BUFFERS

SIZE	CODE IDENT NO		
2	24672	103 99019	
SCALE 2:1			SHEET 1 OF 1

PT. CLARENCE, AK
99900Y

SHOAL COVE, AK
59900X, 79600Y

TOK, AK
79600M

NARROW CAPE, AK
79600X, 99900Z

ST. PAUL IS., AK
99900M

ATTU, AK
99900X

KURE IS., HI
49900Y

UPOLO PT., HI
49900X

JOHNSON IS., HI
49900M

WILLIAMS LAKE, BC
59900M

PORT HARDY, BC
59900Z

GEORGE, WA
99400W, 59900X

FALLON, NV
99400M

MIDDLETOWN, CA
99400X

SEARCHLIGHT, NV
99400Y

RAYMONDVILLE, TEXAS
79800X

GRANGEVILLE, LA
79800W

BAUDETTE, MN
89700Y

DANA, IN
89700M,
99600Z

SANDUR, ICELAND
79300W, 79700Y

ANGISSOQ,
GREENLAND
79300M

CARIBOU, ME
59300M, 99600W

CAPE RACE, NFLD
59300Y, 79300Z

SENCCA, NY 99600M,
89700X

NANTUCKET, MA
59300X, 99600X

CAROLINA BEACH, NC
79800Z, 99600Y

MALONE, FL
79800M, 89700W

JUPITER, FL
79800Y

JAN MAYEN, NORWAY
79700Z

EJDE, FAEROE IS.,
DENMARK
79300X, 79700M

SYLT,
GERMANY
79700W

ESTARTIT, SPAIN
79900Z

LAMPEDUSA, IT
79900X

BO, NORWAY
79700X

SELLIA MARINA, IT
79900M

KARGABARUM, TURKEY
79900Y

POHANG, KOREA
59700M

KWANG JU, KOREA
59700X

HOKKAIDO, JAPAN
99700X, 59700W

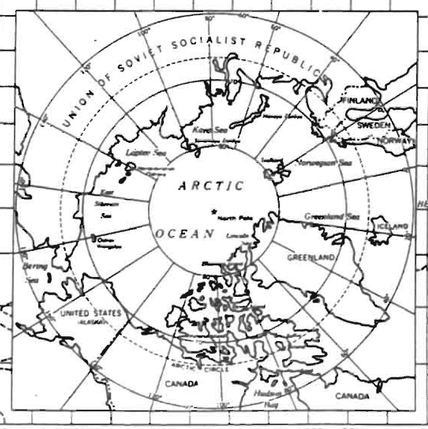
IWO JIMA, JAPAN
99700M

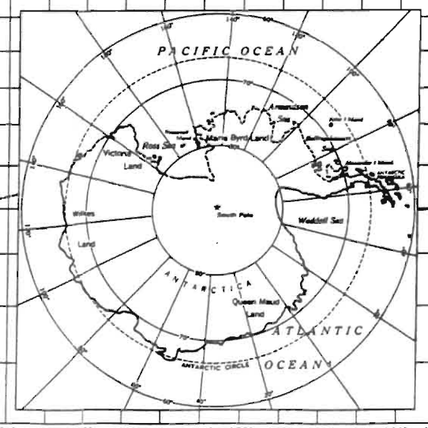
MARCUS IS., JAPAN
99700W

GESASHI, JAPAN
59700Y, 99700Y

YAP IS., USA
99700Z

ARCTIC OCEAN
PACIFIC OCEAN
ATLANTIC OCEAN
INDIAN OCEAN
GREENLAND
CANADA
UNITED STATES
UNION OF SOVIET SOCIALIST REPUBLICS
CHINA
INDIA
AUSTRALIA
MEXICO
BRAZIL
ARGENTINA
PERU
BOLIVIA
SOUTH AFRICA
NEW ZEALAND
MONGOLIA
PHILIPPINES
MALAYSIA
INDONESIA
BERING SEA
HUDSON BAY
GULF OF MEXICO
CARIBBEAN SEA
BARENTS SEA
NORWEGIAN SEA
GREENLAND SEA
SEA OF OKHOTSK
SEA OF JAPAN
BLACK SEA
ARABIAN SEA
BAY OF BENGAL
SCOTIA SEA
WEDDELL SEA
HELLINGSHAUSEN SEA
ANTARCTIC CIRCLE





6.0 MAINTENANCE

6.1 SCOPE OF SECTION

6.1.1 The maintenance section of this manual provides the technician with a general approach to maintaining the Model 2100. Included are trouble analysis guides and alignment procedures.

6.2 TROUBLE ANALYSIS GUIDES

6.2.1 The Model 2100 has several test routines that can be run by the operator if a problem develops. These routines are discussed in detail in the following paragraphs. It must be remembered that if the receiver is tracking or trying to acquire a Loran-C signal, these tests cannot be run. To stop tracking or acquisition, enter zero, then push ACQ.

6.2.2 Considerable lost time and trouble can be avoided by following certain steps before beginning any major troubleshooting procedure. If the Model 2100 is malfunctioning and general testing seems to be in order, go through the following checklist before starting the testing:

1) AC and DC connections secure.
2) External frequency standard connected.
3) Frequency select toggle switch on the MPU/MEMORY pcb is set to the frequency of the external reference. As viewed from the front of the receiver, the 1MHz position is to the left, the 10MHz position is in the center, and the 5MHz position is to the right.
4) Antenna installation is proper and the antenna interconnect cable is secure at both ends.

5) Fuses are intact and of the proper rating.

6) The three power supply voltages are within the following tolerances:

+5 VDC, ±0.25 VDC
+12 VDC, ±0.5 VDC
-12 VDC, ±0.5 VDC

7) It is sometimes helpful to clean the contacts of the printed circuit boards. To do this, turn power off and lower the front panel. Carefully remove each board, lightly clean both sides of the edge connector with a typewriter erasure, and replace in the same slot.

6.2.3 If the problem still exists after performing the checks in paragraph 6.2.2, it will be necessary to run more extensive tests. The following equipment will be necessary to test the Model 2100:

a) Oscilloscope
b) Signature analyzer
c) VOM, Triplett Model 603 or equivalent.

6.2.4 The following procedures should be followed while performing the receiver tests:

WARNING: Line voltages are present on the inside surface of the rear panel (left side, as viewed from the front) and on the transformer.

a) Turn power off when installing or removing PCB assemblies.
b) The +5 V regulator is located on the left side of the chassis and is secured to the side panel by two screws. These screws should be tight while operating under load to prevent overheating.
c) The three large boards in the center of the chassis may be installed in any order to facilitate testing. When a board is to be tested, insert it in the top slot. For normal operation, leave the boards in the order,

1) 1MHz Phase Shifter, P/N 10398083 (top).
2) Acquire/Track, P/N 10398087 (middle).
3) MPU/Memory, P/N 10398079 (bottom).

d) The three analog printed circuit boards are located on the right-hand side of the chassis. The top 2 boards, 1st and 2nd RF Amplifiers, can be installed in either order, with the top position used for troubleshooting. For normal operation, however, the 2nd RF Amplifier should be installed in the upper slot, with the 1st RF Amplifier in the middle slot. The third PCB, A/D Converter, always occupies the bottom position.

e) The Front Panel Display/Keyboard is mounted on standoffs on the back of the front panel. To remove this PCB from the panel, disconnect the two cables and remove the six screws and lockwashers from the back of the PCB. DO NOT disturb the black oxide screws securing the standoffs. Reassemble this PCB and the front panel by reversing this order. Before tightening the six screws, be sure the pushbutton switches do not bind when pushed. Reconnect the ribbon cables. Make sure there are no twists.

6.2.5 The main test procedure for the Model 2100 involves the measurement of circuit "signatures". The signatures are four-digit numbers measured by a signature analyzer at the various nodes of a digital circuit. Programming in the receiver stimulates the nodes in a known way, producing a pattern of ones and zeros. This data sequence is "compressed" by the signature analyzer to produce the signature, which is then compared to the signature determined at the factory and recorded in the manual.

6.2.5.1 The signature at a node must be stable and must be the same as the signature measured at the factory. If it is incorrect or changing, follow the signal back toward its source by measuring signatures at appropriate pins, until a correct signature is found. The

problem will usually be between the correct signature and the last bad signature. This boundary (between bad signature and good signature) will usually occur between the input and output of a gate, flip-flop, buffer, etc. If a logic element has more than 1 input, check the other inputs before deciding that the element is bad. If all other inputs are correct, a visual inspection of the output trace should be made for shorts to other circuit elements.

6.2.5.2 Another fault that can be detected is an open trace. In this case, the signature at the output of a circuit is good, but the input siganture of a device using that signal is bad. Examine the trace visually or with the signature analyzer to find the opening.

6.2.5.3 Each signature table contains the PCB name, the IC pin connections for the CLOCK, START, and STOP signals, and the test to be run. When signatures are to be measured, turn power off, put the PCB to be tested in the top slot, and connect the signature analyzer. Be careful not to short the analyzer connectors to adjacent pins or traces. Before measuring any other signatures, measure the signatures for the +5V line and ground, shown in the upper right-hand corner of the signature table. This will verify the setup of the signature analyzer. Measure the other signatures as specified in the test procedure and compare to the signatures in the appropriate signature table.

6.3 TESTING THE KERNAL

6.3.1 The kernal of the Model 2100 hardware includes the microprocessor, the address lines and the address decoders. If there is a problem with the kernal, the receiver will probably not respond to the function pushbuttons, and the numeric display and LED indicators will flash erratically. All other tests are controlled by programs in the EPROMs so the kernal must be operating properly.

6.3.2 The kernal is tested by setting the rocker switches (S1) on the MPU/Memory circuit board to the TEST position. This disables the bidirectional data buffers, U38 and U40, and forces the 8

microprocessor data lines to the binary code, 01011111. This code causes the MPU to continuously cycle through the entire address field (65,536 addresses). As it does so, all hardware using the MPU address lines is exercised.

6.3.3 Turn receiver power off and install the MPU/Memory PCB in the top slot (exchange slots with the 1MHz Phase Shifter PCB). Set the four rocker switches of S1 to the TEST position. Reconnect the ribbon cable and connect the signature analyzer as outlined in Table 6-1. Turn power on. Measure the signatures at the nodes indicated in Table 6-1 and compare to the correct signatures. Table 6-1 contains a minimal set of signatures that must be checked. If these signatures are correct, the kernal test of this board is complete. If incorrect signatures are found, Table 6-2 shows additional signatures which should help locate the faulty component.

6.3.4 To do the kernal test on the ACQUIRE/TRACK PCB, install this board in the top slot, put the MPU/Memory board in the bottom slot and put the 1MHz Phase Shifter in the middle slot. Be certain the four rocker switches of S1 on the MPU/Memory PCB are set to the TEST position. Connect the analyzer as outlined in Table 6-3. Turn power on and measure the signatures. Measured signatures must be stable and must agree with the correct signatures.

6.3.5 To do the kernal test on the 1MHz Phase Shifter PCB, put it in the top slot and put the ACQUIRE/TRACK PCB in the middle slot. Set the four rocker switches of S1, on the MPU/Memory PCB, to the TEST position. Connect the signature analyzer as outlined in Table 6-4 and measure the signatures. Measured signatures must be stable and must agree with the signatures in the table.

6.4 MODEL 2100 TEST ROUTINES

6.4.1 There are six TEST routines in the Model 2100 that are run on demand. To execute a test, push the TEST function switch, then the number of the test. TEST 0 causes the output of the current revision

TABLE 6-1

REF: MPU/MEMORY (SCHM = 12398080) Vcc = 0003
TEST: KERNAL GND = 0000

CLOCK: U8-1, trigger negative.
START: U25-3, trigger positive.
STOP: U5-8, trigger positive.

DEVICE	P/N	SIGNATURE
P1	7	5P1A
	17	282A
	33	0002
	34	4FCA
	35	6U28
	36	7791
	37	6F9A
	38	1U5P
	39	P763
	40	UUUU
	$\overline{M}$	9UP1
	$\overline{N}$	4868
	$\overline{P}$	37C5
	$\overline{R}$	6321
	$\overline{S}$	U759
	$\overline{T}$	0356
	$\overline{U}$	8484
	$\overline{V}$	FFFF
U11	4	3F6P
	5	OU18
	6	83F5
	7	20U2
	9	8223
	10	0880
	11	220F
	12	883U

DEVICE	P/N	SIGNATURE
U12	7	2093
	9	9042
	10	4135
	11	36A7
	12	A445
	13	464F
	14	4U99
	15	9A4F
U14	6	7792
	8	404H
U23	4	3APP
	5	02H5
	6	282A
	7	5P1A
	9	F4AC
	10	P7AA
	11	132H
	12	HA92
U24	8	H285

TABLE 6-2

REF: MPU/MEMORY (SCHM = 12398080) Vcc = 0003
TEST: KERNAL GND = 0000

CLOCK: U8-1, trigger negative.
START: U25-3. trigger positive.
STOP: U5-8, trigger positive.

DEVICE	P/N	SIGNATURE
U2	8	PACH
	9	0003
	10	9UP1
	11	0002
U6	1	0003
	2	0003
	3	4FC9
	4	486C
	5	9UP2
	6	0001
	8	4P08
	11	0003
	12	0003
U13	8	404P

TABLE 6-3

REF: ACQUIRE/TRACK (SCHM ‡2398088) Vcc = 7A70
TEST: KERNAL GND = 0000

CLOCK: U1-2, trigger positive.
START: U48-18, trigger positive.
STOP: U48-19, trigger positive.

DEVICE	P/N	SIGNATURE
U1	3	6F95
	6	F300
	8	H233
U48	1	H233
	2	1060
	3	AOU4
	4	OFH1
	5	67H8
	6	7H1A
	7	CCAA
	8	0A06
	9	266H
	10	PH77
	11	9UC1
	13	F300
	14	142F
	15	21P7
	16	6F95
	17	UUF9
	18	0000
	19	8P54
	20	P030
	21	H0AA
	22	HA07
	23	C21A

TABLE 6-4

REF: 1 MHz PHASE SHIFTER (SCHM = 12398084) Vcc = 7A70
TEST: KERNAL GND = 0000

CLOCK: U38-2, trigger positive.
START: U40-18, trigger negative.
STOP: U40-19, trigger negative.

DEVICE	P/N	SIGNATURE
U38	11	0A06
U40	7	CCAA
	8	0A06
	9	266H
	11	9UC1
	13	F300
	18	0000
	19	8P54
	20	P030
	21	H0AA
	22	HA07
	23	C21A

level of the receiver software. Before turning power on, be sure the four rocker switches of S1, on the MPU/Memory PCB are in the NORMAL position.

6.4.2 Most of the TEST routines will terminate automatically when completed. Others must be terminated by the operator. During execution of a test, the TEST LED will be on.

6.4.3 TEST 1 -- This test exercises the front panel numeric display and LED indicators. When the test begins, the left-hand digit of the liquid crystal display begins incrementing from zero. All other digits are blank. When 9 is reached, the digit is blanked and the next digit to the right is incremented. This continues until all 8 digits have been cycled. Be sure each digit increments correctly, there are no missing (or continusouly on) segments, only 1 digit is incremented at a time, and the test proceeds from left to right. Occasionally, the display will become loose in the socket causing 1 or more segments to fail (usually they will stay on). To correct this, the front panel PCB can be removed from the panel and the display reseated. Use only light pressure to avoid breaking the display and possibly causing personal injury.

6.4.3.1 After the liquid crystal display is tested, the LED indicators for TRACKING (2 color LED), SETTLE, ACQUIRE, BLINK, CYCLE, and TEST are turned off and on together about once a second. This continues for about 5 seconds. Check all LEDs for proper operation. The TRACKING LED will appear yellow or yellow-orange, indicating that both the red and green LEDs are on.

6.4.3.2 The next indicators tested are the units LEDs (USEC, CYCLE, and dB) and the liquid crystal symbols, decimal point, colons, and minus sign. They are flashed for about 5 seconds. There should be 2 colons and 1 decimal point.

6.4.4 TEST 2 -- This test checks the operation of the front panel pushbutton switches. Once this test is started it must be terminated by the operator. During the test, push each of the pushbuttons on the front panel. The numeric display will show a 2 digit number for each switch, as shown below:

SWITCH	DISPLAY	SWITCH	DISPLAY	SWITCH	DISPLAY
0	00	9	09	SECOND	18
1	01	.	10	MASTER	19
2	02	+/-	11	SEC.TD.	20
3	03	CLEAR	12	GRI	21
4	04	TEST	13	BEGIN TOC	22
5	05	SCAN STROBE	14	FIRST TOC	23
6	06	TRACK DATA	15	TOC ADJUST	24
7	07	0/FS	16	UTC	25
8	08	RANGE	17	1PPS SLEW	26

To terminate the test, push the BACKLIGHT pushbutton. If the display changes to the GRI and the TEST LED goes out, this key is working properly.

6.4.5 TEST 3 -- This test checks the 2048-words by 8-bits, random access memory (RAM) on the MPU/Memory PCB. The RAM consists of 4 integrated circuits, each of which contains 1024 locations, 4 bits wide. U27 and U28, together, form the upper 1024 8-bit words and U25 and U26 form the lower 1024 8-bit words (U25 and U27 are connected to MPU data lines, D4-D7, and U26 and U28 are connected to MPU data lines, D0-D3).

6.4.5.1 When the test is run, the display will be, E1XXYYYY. E1 indicates the RAM test. If the RAM is good, XX will be 00 and YYYY will 2048. If a problem is detected, YYYY will be the decimal address of the first memory location found to be bad. For memory locations 0000

through 1023, U25 and/or U26 may be bad; for locations 1024 through 2047, U27 and/or U28 may be bad. Use the following table to determine the bad IC:

XX	YYYY	PROBABLE IC
00	2048	RAM good
01,10,11	2048	Not possible
01	0000-1023	U25 may be bad
01	1024-2047	U27 may be bad
10	0000-1023	U26 may be bad
10	1024-2047	U28 may be bad
11	0000-1023	U25 & U26 may be bad
11	1024-2047	U27 & U28 may be bad

6.4.5.2 Before changing an integrated circuit, it may be helpful to examine the RAM select lines, $\overline{WE}$ and $\overline{CS}$. If these inputs do not change between a logic 1 and a logic 0 when the test is run, the problem may be in the RAM select circuitry. The kernal test described in section 6.3.3 should be run.

6.4.5.3 If one or more RAM ICs are changed, the test should be run again. Another IC may be bad, but, because of its position in memory, it will not be detected until the earlier problems are solved.

6.4.6 TEST 4 -- This test checks the erasable programmable read only memory (EPROM), U41, U42, and U43. An output of "E-20" indicates a properly functioning EPROM. An output of "E-21" indicates that one or more of the EPROMs are bad. The quickest solution is to replace the 3 EPROMs with new (programmed) ICs. If this does not correct the problem, there may be a problem with the EPROM select circuitry.

6.4.6.1 To change an EPROM, remove the EPROM from its socket and insert the new one. Be careful that the AUSTRON part number on the new EPROM matches the number on the old part. Check for any bent pins on the new EPROM.

6.4.7 TEST 5 -- TEST 5 generates the necessary receiver signals to calibrate the digital-to-analog converters (DAC) on the 1MHz

PHASE SHIFTER PCB and the ACQUIRE/TRACK PCB (AUSTRON P/N, 10398083 and 10398087). Avoid making unnecessary adjustments to these circuit boards. They should require adjustment only when a DAC is replaced.

6.4.7.1 With power off, put one of the two printed circuit boards in the top slot and the other in the middle slot. Turn power on and push TEST 5.

1) 1 MHz PHASE SHIFTER CALIBRATION (10398083)

a) Connect the oscilloscope to U31 pin 5 and trigger on the positive transition of the signal. The TTL level signal at this node will be a 500KHz pulse, with a high level pulse width changing by about 1 μsec, from minimum to maximum. Adjust R19 so that the difference between the short and long periods (measured half-way up on the pulse) is 985 nsec ±5 nsec. This same differential should appear at U31 pin 13 (it may differ by about 20 nsec).

b) Connect the oscilloscope to U20 pin 5 and trigger on the positive transition of the signal. The TTL level signal at this node will be switching at 1MHz, with the logic 1 level changing by about 0.5 microsecond, from minimum to maximum. Adjust R32 so that the difference between the short and long periods is 490 nsec ±5 nsec.

c) Turn power off. Connect the oscilloscope to U1 pin 5. Turn power on. Do not execute TEST 5. The signal at this point should be a 1MHz square wave. Set the oscilloscope timebase to show 1 cycle and trigger on the positive transition. Adjust R8 to minimize the double edge at the right side of the oscilloscope graticule.

d) Connect the oscilloscope to U3 pin 5. The output should be a 1MHz square wave. Set the oscilloscope timebase to show one cycle and adjust R27 to minimize the double edge at the right side of the oscilloscope graticule.

2) ACQUIRE/TRACK CALIBRATION (10398087)

a) Turn power off and put the ACQUIRE/TRACK PCB in the top slot. Connect the oscilloscope to U28 pin 18. Turn power on and execute TEST 5. This output should be switching between zero volt and one volt (±0.05V).

b) Connect the oscilloscope to U43 pin 18. The signal should be changing between zero and ±5 volts - ±0.5 volt.

c) Connect the oscilloscope to U40B pin 5 and trigger on the positive going edge of the 1MHz signal. The high level period of the signal should be changing and should be adjusted for a difference of 490 nsec ±5 nsec. Adjust R21 as necessary.

6.4.8 TEST 6 -- TEST 6 provides the necessary stimulus to measure the signatures at the outputs of various latches in the receiver. Put the PCB to be tested in the top slot and connect the signature analyzer according to the table of signatures (shown below).

6.4.8.1 To measure the signatures on the 1MHz PHASE SHIFTER PCB using TEST 6, connect the signature analyzer according to Table 6-5. Turn power on and execute TEST 6. Measure the signatures and compare to the correct signatures in the table.

6.4.8.2 To measure the signatures on the ACQUIRE/TRACK PCB using TEST 6, connect the signature analyzer according to Table 6-6.

TABLE 6-5

REF: 1 MHz PHASE SHIFTER (SCHM = 12398084) Vcc = 0068
TEST: #6 GND = 0000

CLOCK: U38-2, trigger positive.
START: U39-12, trigger positive.
STOP: U38-9, trigger positive.

DEVICE	P/N	SIGNATURE
U12	3	7361
	5	H16U
U38	8	A542 or 4A3H
U39	2	UFP6
	5	6866
	6	H82A
	9	58UF
	11	HU29
	12	225C
	15	3762
	16	A365
	19	0012

TABLE 6-6

REF: ACQUIRE/TRACK (SCHM = 12398088) Vcc = 0068
TEST: #6 GND = 0000

CLOCK: U1-9, trigger positive.
START: U34-12, trigger positive.
STOP: U45-13, trigger positive.

DEVICE	P/N	SIGNATURE
U3	9	P45U
U27	2	9HP8
	5	F882
	6	7508
	9	4HU3
	11	6PUP
	12	182A
	15	6175
	16	0C57
	19	FU25
U34	2	4U19
	5	58UF
	6	H82A
	9	6866
	11	P892
	12	225C
	15	3762
	16	A365
	19	0012
U35	2	H479
	5	36U3
	6	A940
	9	6U59
	11	219P
	12	0A12
	15	3APC
	16	8U46
	19	CCU3
U48	1	A830
	5	P892
	6	219P
	7	2F30
	10	6PUP
	14	5209
	15	8096
	18	A8P7
	19	446F
	20	43C6
	21	AF08
	22	P5C6
	23	5UPF

Turn power on and execute TEST 6. Measure the signatures and compare to the correct signatures in the table.

6.4.8.3 Additional circuits on the ACQUIRE/TRACK PCB should also be checked at this time. Terminate TEST 6 by turning power off. Connect the signature analyzer as shown in Table 6-7 and turn power on. Make sure the Group Repetition Rate (GRI) is set to 65536 μsec. Measure the signatures at the nodes shown in Table 6-7.

TABLE 6-7

REF: ACQUIRE/TRACK (SCHM = 12398088) Vcc = 0001
TEST: NO TEST, SET GRI = 65536 GND = 0000

CLOCK: U3-3, trigger positive.
START: U21-3, trigger positive.
STOP: U18-6, trigger positive.

DEVICE	P/N	SIGNATURE
P1	12	64FC
	18	C74U
	S	5F74
	U	3U5A
	$\overline{E}$	9P8F
	$\overline{F}$	483A
U3	5	UUUP
	6	UUUU
U4	8	UUUP
	11	7F4H
U8	3	A3A8
	7	12UC
	9	CHPU
U9	4	7F4F
	6	P426
	8	C6C0
	10	FOUA
	11	H936
U10	6	421P
	8	421U
U44	3	5AP1
	4	CHF1
	5	2526
	6	C5FU
	8	0001
	9	PACP
U44	10	704U
	11	772F
U47	3	AAAA
	4	7777
	5	U8U8
	6	CA42
	8	C713
	9	A591
	10	UH9C
	11	1594

DEVICE	P/N	SIGNATURE
U11	3	H718
	6	0000
	8	0001
	10	0001
	11	0001
U12	8	HUC7
	9	HUC6
U19	5	F631
	8	3U5C
	9	3U5A
U20	5	C74U
U21	5	0001
	8	8001
U22	5	73F0
	6	73F1
	9	8AA9
U23	8	5F75

7.0 PARTS LISTS

7.1 SCOPE OF SECTION

7.1.1 This section contains lists of replaceable parts which include the reference designator, the part description, and the AUSTRON part number. For convenience in ordering from local suppliers, the manufacturer's part number and the manufacturer's Federal Identification Code (FIC) are also given where applicable.

7.2 ORDERING REPLACEMENT PARTS

7.2.1 To order replacement parts from AUSTRON, Inc., address the order to:

AUSTRON, INC.
1915 Kramer Lane
Austin, Texas 78758

Specify for each part, the AUSTRON part number, revision letter, part description, circuit reference designator, and the printed circuit board on which the part is located. To order parts not listed in this section give a complete description of the function of the part and its location in the unit. Along with each order, add the model and serial numbers of the unit, which can be found on a label attached to the rear panel.

7.2.2 Manufacturer part numbers as shown will change occasionally as vendor items are re-evaluated or as improved components become available. The equivalent part currently used in production at the time orders are received will be shipped. Where the manufacturer's part number or FIC is missing, any reputable manufacturer's part of the appropriate value, indicated in the description, may be used.

7.2.3 The circuit reference designator includes the reference designator prefix in the page heading plus the reference designator for the individual part. If, for example, the reference designator prefix for a circuit board assembly is 1A4A7 and the desired component is capacitor C1, the complete circuit reference designator would be 1A4A7C1.

NOTE: Parts location diagrams are included in section 5.0. Parts lists are assembled within this section in reference designator order.

ASSEMBLY LORAN-C TIMING RECEIVER MODI 2100
ASSEMBLY NUMBER 30498041
REFERENCE DESIGNATOR PREFIX 1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
	FUSE 3AG 1 AMP 250V	552001-0019	312001	75915
	FUSE 3AG 2 AMP 250V	552001-0024	312002	75915
	CONN, STRAIGHT 3 SOCKET CONTACT	551106-0017	MS3106A-14S-1S	96906
	CLAMP, AN3057-6	551013-0006	AN3057-6	81352
A1	FINAL ASSY LORAN-C TIMING RECEIVER	25498042		24672
W1	POWER CORD, (SPECIAL)	570076-0002	17250	70903

ASSEMBLY FINAL ASSY LORAN-C TIMING RECEIVER
ASSEMBLY NUMBER 25498042
REFERENCE DESIGNATOR PREFIX 1A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	PCB ASSY FRONT PANEL LCD DIS/KEY	10398598		24672
A2	PCB ASSY INTERCONNECT	10398026		24672
A2A1	PCB ASSY 1ST RF AMP	10398067		24672
A2A2	PCB ASSY 2ND RF AMPLIFIER	10398071		24672
A2A3	PCB ASSY ADC/SAMPLE HOLD	10398075		24672
A2A4	PCB ASSY 1 MHZ PHASE SHIFTER	10398083		24672
A2A5	PCB ASSY ACQUIRE/TRACK	10398087		24672
A2A6	PCB ASSY MPU/MEMORY	10398079		24672
A2A7	PCB ASSY +5 VOLT REGULATOR	10398059		24672
A3	OPT 01 IEEE-488(GPIB) INTERFACE	12898484		24672
A3A1	PCB ASSY GENL PURP INTERFACE BUS	10398250		24672
A3	PCB ASSY ADC/SAMPLE HOLD	10398075		24672
A4	PANEL ASSY REAR	10998047		24672

ASSEMBLY PCB ASSY FRONT PANEL LCD DIS/KEY
ASSEMBLY NUMBER 10398598
REFERENCE DESIGNATOR PREFIX 1A1A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C2	1 UF 35V 10 CAP TANT	608017-0105	CS13BF105K	81349
C3	.001 UF 100V 20 CAP CERAFIL	601205-0102	CK12BX102M	81349
C4	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C5	1 UF 35V 10 CAP TANT	608017-0105	CS13BF105K	81349
DS1	LUMINESCENT LCD BACK LIGHT	555700-0001	0554-1232	32890
DS2	LCD 8-DIGIT 1/2" CHAR(SEE SPEC SHT)	555700-0002	P5580-M3	00000
DS3	3.0 MCD 20MA T1 3/4 LED GRN	555600-4955	5082-4955	28480
DS4	LED MULTICOLOR (RED/GREEN)	555505-0091	521-9178	13812
DS5	2.5 MCD 10MA T1 LED RED HI EFF	555600-4684	HLMP1301	28480
DS6	2.5 MCD 10MA T1 LED RED HI EFF	555600-4684	HLMP1301	28480
DS7	2.5 MCD 10MA T1 LED RED HI EFF	555600-4684	HLMP1301	28480
DS8	LED MULTICOLOR (RED/GREEN)	555505-0091	521-9178	13812
DS9	2.0 MCD 10MA T1 3/4 LED RED HI EFF	555600-4650	5082-4650	28480
DS10	2.0 MCD 10MA T1 3/4 LED RED HI EFF	555600-4650	5082-4650	28480
DS11	2.0 MCD 10MA T1 3/4 LED RED HI EFF	555600-4650	5082-4650	28480
DS12	2.0 MCD 10MA T1 3/4 LED RED HI EFF	555600-4650	5082-4650	28480
DS13	2.0 MCD 10MA T1 3/4 LED RED HI EFF	555600-4650	5082-4650	28480
P1	CONN 26 PIN	551107-6626	87215-9	00779
Q1	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
R1	1 K 1/8W 10 RES FXD COMP	651110-0102	RC05GF102K	81349
R2	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R3	150 OHM 1/8W 10 RES FXD COMP	651110-0151	RC05GF151K	81349
R4	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R5	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R6	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R7	150 OHM 1/8W 10 RES FXD COMP	651110-0151	RC05GF151K	81349
R8	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R9	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R10	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R11	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349
R12	4.7 K 1/8W 10 RES FXD COMP	651110-0472	RC05GF472K	81349
R13	470 OHM 1/8W 10 RES FXD COMP	651110-0471	RC05GF471K	81349

ASSEMBLY PCB ASSY FRONT PANEL LCD DIS/KEY (CONT)
ASSEMBLY NUMBER 10398598
REFERENCE DESIGNATOR PREFIX 1A1A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R14	270 OHM 1/8W 10 RES FXD COMP	651110-0271	RC05GF271K	81349
S1	SWITCH, PUSHBUTTON, SPST, PLAIN BLK	553909-0012	320.22 E1-1 BLK	00000
S2	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S3	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S4	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S5	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S6	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S7	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S8	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S9	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S10	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S11	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S12	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S13	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S14	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S15	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S16	SWITCH, PUSHBUTTON, SPST, PLAIN WHT	553909-0013	320.22 E1-1	00000
S17	SWITCH, PUSHBUTTON, SPST (7)	553909-0007	320 E1-1	00000
S18	SWITCH, PUSHBUTTON, SPST (8)	553909-0008	320 E1-1	00000
S19	SWITCH, PUSHBUTTON, SPST (9)	553909-0009	320 E1-1	00000
S20	SWITCH, PUSHBUTTON, SPST (4)	553909-0004	320 E1-1	00000
S21	SWITCH, PUSHBUTTON, SPST (5)	553909-0005	320 E1-1	00000
S22	SWITCH, PUSHBUTTON, SPST (6)	553909-0006	320 E1-1	00000
S23	SWITCH, PUSHBUTTON, SPST (1)	553909-0001	320 E1-1	00000
S24	SWITCH, PUSHBUTTON, SPST (2)	553909-0002	320 E1-1	00000
S25	SWITCH, PUSHBUTTON, SPST (3)	553909-0003	320 E1-1	00000
S26	SWITCH, PUSHBUTTON, SPST (0)	553909-0000	320 E1-1	00000
S27	SWITCH, PUSHBUTTON, SPST (.)	553909-0010	320 E1-1	00000
S28	SWITCH, PUSHBUTTON, SPST (+/-)	553909-0011	320 E1-1	00000
U1	IC CMOS QUADR 2-INP EXCL-OR GATE	703MM74C86N	MM74C86N	40948
U2	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U3	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U4	IC CMOS 20 KEY KEYBOARD ENCODER	703MM74C923N	MM74C923N	40948

ASSEMBLY PCB ASSY FRONT PANEL LCD DIS/KEY (CONT)
ASSEMBLY NUMBER 10398598
REFERENCE DESIGNATOR PREFIX 1A1A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U5	IC OCTAL BUFFER LINE DRVR/RCVR	703SN74LS244	SN74LS244N	01295
U6	IC CMOS 20 KEY KEYBOARD ENCODER	703MM74C923N	MM74C923N	40948
U7	IC CMOS 4 DIGIT DISPLAY DECODER	703ICM7211AM	ICM7211AMIPL	32293
U8	IC CMOS 4 DIGIT DISPLAY DECODER	703ICM7211AM	ICM7211AMIPL	32293
W1	CABLE ASSY 10 CONDUCTOR	12098805		24672

ASSEMBLY PCB ASSY INTERCONNECT
ASSEMBLY NUMBER 10398026
REFERENCE DESIGNATOR PREFIX 1A1A2
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	8700 UF 40 V 10 CAP ELEC	602036-0878	36DX872G040AC2A	56289
C2	15 UF 20 V 10 CAP TANT	608016-0156	CS13BF156K	81349
C3	15 UF 20 V 10 CAP TANT	608016-0156	CS13BF156K	81349
CR1	100VR 5A DIO S RECT	701A15A	A15A	03508
CR2	100VR 5A DIO S RECT	701A15A	A15A	03508
CR3	100VR 5A DIO S RECT	701A15A	A15A	03508
CR4	100VR 5A DIO S RECT	701A15A	A15A	03508
CR5	500VR 12A DIO S RECT DO-4	701MR1125	MR1125	04713
L1	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
L2	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
L3	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
P1	CONN 26 PIN	551107-6626	87215-9	00779
R1	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
T1	XFMR POWER 28V 2 AMP	751310-0001	DSB82B	
U1	CONVERTER, DC/DC	570901-0210	BPM-12/210-D5	50721
XA1	CONN 12PIN DUAL READOUT PC TAB	551009-0013	6007-024-451-012	11769
XA2	CONN 12PIN DUAL READOUT PC TAB	551009-0013	6007-024-451-012	11769
XA3	CONN 12PIN DUAL READOUT PC TAB	551009-0013	6007-024-451-012	11769
XA4	CONN DUAL 43/86 PIN SOLDER TAIL	551108-0018	ESM43DTKI	54453
XA5	CONN DUAL 43/86 PIN SOLDER TAIL	551108-0018	ESM43DTKI	54453
XA6	CONN DUAL 43/86 PIN SOLDER TAIL	551108-0018	ESM43DTKI	54453
XA7	CONN 10PIN DUAL READOUT PC TAB	551009-0002	50-20B-10	71785

ASSEMBLY PCB ASSY 1ST RF AMP
ASSEMBLY NUMBER 10398067
REFERENCE DESIGNATOR PREFIX 1A1A2A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C2	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C3	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C4	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C5	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C6	1200 PF 100V 5 CAP DIP MICA	603000-0122	DM15-122J	72136
C7	1500 PF 500V 5 CAP DIP MICA	603000-0152	DM19-152J	72136
C8	150 PF 500V 5 CAP DIP MICA	603000-0151	DM15-151J	02799
C9	560 PF 300V 5 CAP DIP MICA	603000-0561	DM15-561J	72136
C10	18 PF 500V 5 CAP DIP MICA	603000-0180	DM15-180J	72136
C11	270 PF 500V 5 CAP DIP MICA	603000-0271	DM15-271J	72136
C12	18 PF 500V 5 CAP DIP MICA	603000-0180	DM15-180J	72136
C13	330 PF 500V 5 CAP DIP MICA	603000-0331	DM15-331J	02799
C14	910 PF 500V 5 CAP DIP MICA	603000-0911	DM15-9110	72136
C15	1200 PF 100V 5 CAP DIP MICA	603000-0122	DM15-122J	72136
C16	390 PF 500V 5 CAP DIP MICA	603000-0391	DM15-391J	72136
C17	4700 PF 200V 10 CAP CERAMIC	601105-0472	CN30A472K	71590
C18	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C19	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C20	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C21	39 PF 500V 5 CAP DIP MICA	603000-0390	DM15-390J	72136
C22	1500 PF 500V 5 CAP DIP MICA	603000-0152	DM19-152J	72136
C23	75 PF 500V 5 CAP DIP MICA	603000-0750	DM15-750J	72136
C24	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C25	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C26	10 UF 20 V 10 CAP TANT	608016-0106	CS13BE106K	81349
C27	10 UF 20 V 10 CAP TANT	608016-0106	CS13BE106K	81349
C28	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C29	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C30	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C31	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C32	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C33	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590

ASSEMBLY PCB AcSY 1ST RF AMP (CONT)
ASSEMBLY NUMBFR 10398067
REFERENCE DESIGNATOR PREFIX 1A1A2A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C34	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C35	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C36	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C37	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C38	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C39	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C40	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C41	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
L1	3900 UH 10 INDUCTOR VARIABLE	751150-0392	VLS-392	72259
L2	10000 UH 10 INDUCTOR VARIABLE	751150-0103	WEE-VL-10000	72259
L3	8200 UH 10 INDUCTOR VARIABLE	751150-0822	WEE-V-L 8200	72259
L4	1500 UH 10 INDUCTOR VARIABLE	751150-0152	WEE-V-L 1500	72259
L5	560 UH 10 INDUCTOR VARIABLE	751150-0561	WEE-V-L 560	72259
L6	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
L7	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
R1	1.87K 1/8W 1 RES FXD FILM	653001-1871	RN55D1871F	81349
R2	1.87K 1/8W 1 RES FXD FILM	653001-1871	RN55D1871F	81349
R3	6.65K 1/8W 1 RES FXD FILM	653001-6651	RN55D6651F	81349
R4	8.2 K 1/4W 10 RES FXD COMP	651102-0822	RC07GF822K	81349
R5	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R6	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R7	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R8	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R9	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R10	150 OHM 1/8W 1 RES FXD FILM	653001-1500	RN55D1500F	81349
R11	150 OHM 1/8W 1 RES FXD FILM	653001-1500	RN55D1500F	81349
R12	2 K 1/8W 1 RES FXD FILM	653001-2001	RN55D2001F	81349
R13	2.49K 1/8W 1 RES FXD FILM	653001-2491	RN55D2491F	81349
R14	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R15	1.87K 1/8W 1 RES FXD FILM	653001-1871	RN55D1871F	81349
R16	1.87K 1/8W 1 RES FXD FILM	653001-1871	RN55D1871F	81349
R17	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R18	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349

ASSEMBLY PCB ASSY 1ST RF AMP (CONT)
ASSEMBLY NUMBER 10398067
REFERENCE DESIGNATOR PREFIX 1A1A2A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R19	10 K 1/8W 1 RES FXD FTI M	653001-1002	RN55D1002F	81349
R20	8.66K 1/8W 1 RES FXD FTI M	653001-8661	RN55D8661F	81349
R21	10 K 1/8W 1 RES FXD FTI M	653001-1002	RN55D1002F	81349
R22	150 OHM 1/8W 1 RES FXD FTI M	653001-1500	RN55D1500F	81349
R23	1.5 K 1/8W 1 RES FXD FTI M	653001-1501	RN55D1501F	81349
R24	10 OHM 1/8W 1 RES FXD FTI M	653001-1009	RN55D1009F	81349
T1	TRANSFORMER RF INPUT	75198399		24672
U1	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U2	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U3	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U4	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U5	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U6	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U7	IC CMOS QUAD SPST ANALOG SWITCH	703HI-201-5	HI-201	34371

ASSEMBLY PCB ASSY 2ND RF AMPLIFIER
ASSEMBLY NUMBER 10398071
REFERENCE DESIGNATOR PREFIX 1A1A2A2
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C2	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C3	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C4	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C5	39 PF 500V 5 CAP DIP MICA	603000-0390	DM15-390J	72136
C6	22 PF 500V 5 CAP DIP MICA	603000-0220	DM15-220J	02799
C7	15P 500V 5 CAP DIP MICA	603000-0150	DM15-015J	72136
C8	10 PF 500V 5 CAP DIP MICA	603000-0100	DM15-100J	02799
C9	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C10	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C11	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C12	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C13	.01 UF 50 V 20 CAP CERAMIC	601100-0103	CY15C103M	71590
C14	27 PF 500V 5 CAP DIP MICA	603000-0270	DM15-270J	02799
C15	75 PF 500V 5 CAP DIP MICA	603000-0750	DM15-750J	72136
C16	.047 UF 250V 5 CAP POLYCARBONATE	610008-0473	B32540C/.047/5/250	25088
C17	.047 UF 250V 5 CAP POLYCARBONATE	610008-0473	B32540C/.047/5/250	25088
C18	.047 UF 250V 5 CAP POLYCARBONATE	610008-0473	B32540C/.047/5/250	25088
C19	.047 UF 250V 5 CAP POLYCARBONATE	610008-0473	B32540C/.047/5/250	25088
C20	10 UF 20 V 10 CAP TANT	608016-0106	CS13BF106K	81349
C21	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C22	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C23	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C24	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C25	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C26	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C27	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C28	10 UF 20 V 10 CAP TANT	608016-0106	CS13BF106K	81349
C29	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C30	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C31	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C32	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C33	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590

ASSEMBLY PCB ASSY 2ND RF AMPLIFIER (CONT)
ASSEMBLY NUMBER 10398071
REFERENCE DESIGNATOR PREFIX 1A1A2A2
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C34	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C35	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
L1	27 UH 10 INDUCTOR VARIABLE	751150-0270	WEE-V-L 27	72259
L2	33000 UH 10 INDUCTOR VARIABLE	751150-0333	WEE-V-L 33000	72259
L3	27 UH 10 INDUCTOR VARIABLE	751150-0270	WEE-V-L 27	72259
L4	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
L5	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
R1	1.87K 1/8W 1 RES FXD FILM	653001-1871	RN55D1871F	81349
R2	1.87K 1/8W 1 RES FXD FILM	653001-1871	RN55D1871F	81349
R3	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R4	17.8K 1/8W 1 RES FXD FILM	653001-1782	RN55D1782F	81349
R5	38.3K 1/8W 1 RES FXD FILM	653001-3832	RN55D3832F	81349
R6	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R7	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R8	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R9	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R10	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R11	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R12	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R13	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R14	5.62K 1/8W 1 RES FXD FILM	653001-5621	RN55D5621F	81349
R15	14.7K 1/8W 1 RES FXD FILM	653001-1472	RN55D1472F	81349
R16	33.2K 1/8W 1 RES FXD FILM	653001-3322	RN55D3322F	81349
R17	71.5K 1/8W 1 RES FXD FILM	653001-7152	RN55D7152F	81349
R18	10 OHM 1/4W 10 RES FXD COMP	651102-0100	RC07GF100K	81349
R19	1 K 1/8W 1 RES FXD FILM	653001-1001	RN55D1001F	81349
R20	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R21	422 OHM 1/8W 1 RES FXD FILM	653001-4220	RN55D4220	51689
R22	422 OHM 1/8W 1 RES FXD FILM	653001-4220	RN55D4220	51689
R23	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R24	56 OHM 1/8W 10 RES FXD COMP	651110-0560	RC05GF560K	81349
R25	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R26	3.48K 1/8W 1 RES FXD FILM	653001-3481	RN55D3481F	81349

ASSEMBLY PCB ASSY 2ND RF AMPlIFIER (CONT)
ASSEMBLY NUMBER 10398071
REFERENCE DESIGNATOR PREFIX 1A1A2A2
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U1	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U2	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U3	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U4	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U5	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U6	IC VOLTAGE COMPARATORS	703LM311H	LM311H	27014
U7	IC CMOS QUAD SPST ANALOG SWITCH	703HI-201-5	HI-201	34371

ASSEMBLY PCB ASSY ADC/SAMPLE HOLD
ASSEMBLY NUMBER 10398075
REFERENCE DESIGNATOR PREFIX 1A1A2A3
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	1000 PF 100V 5 CAP DIP MTCA	603000-0102	CM05FA102J03	81349
C2	3300 PF 500V 5 CAP CERAMIC	601105-0332	CN30-A332K	81349
C3	1000 PF 100V 5 CAP DIP MTCA	603000-0102	CM05FA102J03	81349
C4	.001 UF 250V 10 CAP POLYCARBONATE	610008-0102	B32540C/.001/10/250	25088
C5	.001 UF 250V 10 CAP POLYCARBONATE	610008-0102	B32540C/.001/10/250	25088
C6	.001 UF 250V 10 CAP POLYCARBONATE	610008-0102	B32540C/.001/10/250	25088
C7	22 PF 500V 5 CAP DIP MTCA	603000-0220	DM15-220J	02799
C8	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C9	4.7 UF 35V 10 CAP TANT	608017-0475	CS13BF475K	81349
C10	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C11	4.7 UF 35V 10 CAP TANT	608017-0475	CS13BF475K	81349
C12	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C13	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C14	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
L1	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
L2	WIDEBAND CHOKE	751102-0000	VK20010/3B	02114
R1	27 K 1/4W 10 RES FXD COMP	651102-0273	RC07GF273K	81349
R2	1.5 K 1/4W 10 RES FXD COMP	651102-0152	RC07GF152K	81349
R3	8.2 K 1/4W 10 RES FXD COMP	651102-0822	RC07GF822K	81349
R4	27 K 1/4W 10 RES FXD COMP	651102-0273	RC07GF273K	81349
R5	100 OHM 1/4W 10 RES FXD COMP	651102-0101	RC07GF101K	81349
R6	8.2 K 1/4W 10 RES FXD COMP	651102-0822	RC07GF822K	81349
R7	8.2 K 1/4W 10 RES FXD COMP	651102-0822	RC07GF822K	81349
R8	100 OHM 1/4W 10 RES FXD COMP	651102-0101	RC07GF101K	81349
R9	8.2 K 1/4W 10 RES FXD COMP	651102-0822	RC07GF822K	81349
U1	IC QUADR 2-INP POS-AND GATE	703SN74LS08N	SN74LS08N	01295
U2	IC CMOS QUAD SPST ANALOG SWITCH	703HI-201-5	HI-201	34371
U3	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U4	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U5	IC QUAD D-TYPE FLIP-FLOP	703SN74LS175	SN74LS175N	01295
U6	IC SAMPLE AND HOLD GATED OP AMP	703HA-2425	HA1-2425-5	34371
U7	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U8	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324

ASSEMBLY PCB ASSY ADC/SAMPLE HOLD (CONT)
ASSEMBLY NUMBER 10398075
REFERENCE DESIGNATOR PREFIX 1A1A2A3
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U9	IC 12 BIT A/D CONVERTER	703ADC80712	AD-ADC80Z-12	24355
U10	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U11	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U12	IC SAMPLE AND HOLD GATED OP AMP	703HA-2425	HA1-2425-5	34371
U13	IC SAMPLE AND HOLD GATED OP AMP	703HA-2425	HA1-2425-5	34371

ASSEMBLY PCB ASSY 1 MHZ PHASE SHIFTER
ASSEMBLY NUMBER 10398083
REFERENCE DESIGNATOR PREFIX 1A1A2A4
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C2	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C3	100 PF 500V 5 CAP DIP MICA	603000-0101	DM15-101J	02799
C4	100 PF 500V 5 CAP DIP MICA	603000-0101	DM15-101J	02799
C5	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C6	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C7	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C8	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C9	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C10	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C11	47 PF 500V 5 CAP DIP MICA	603000-0470	DM15-470J	02799
C12	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C13	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C14	2200PF 50V 10 CAP CERAMIC	601105-0222	CN30A-222K	81349
C15	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C16	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C17	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C18	.001 UF 100V 20 CAP CERAFTI	601205-0102	CK12BX102M	81349
C19	47 PF 500V 5 CAP DIP MICA	603000-0470	DM15-470J	02799
C20	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C21	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C22	.22 UF 35V 10 CAP TANT	608017-0224	CS13BF224K	81349
C23	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C24	10 PF 500V 5 CAP DIP MICA	603000-0100	DM15-100J	02799
C25	5.5-18PF CAP VAR CERA	609000-4004	538-011A-5.5-18	72982
C26	.001 UF 100V 10 CAP CERAMIC	601105-0102	CN20A102K	71590
C27	.001 UF 100V 10 CAP CERAMIC	601105-0102	CN20A102K	71590
C28	3.3 UF 15V 10	608015-0335	CS13BD335K	81349
C29	3.3 UF 15V 10	608015-0335	CS13BD335K	81349
C30	.001 UF 250V 10 CAP POLYCARBONATE	610008-0102	B32540C/.001/10/250	25088
C31	330 UF 6 V 10 CAP TANT	608013-0337	CS13BB337K	81349
C32	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C33	100 UF 20 V 10 CAP TANT	608016-0107	CS13BF107K	81349

ASSEMBLY PCB Assy 1 MHZ PHASE SHIFTER (CONT)
ASSEMBLY NUMBER 10398083
REFERENCE DESIGNATOR PREFIX 1A1A2A4
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C34	100 UF 20 V 10 CAP TANT	608016-0107	CS13BE107K	81349
C35	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C36	3.3 UF 15V 10	608015-0335	CS13BD335K	81349
C37	220 PF 100V 10 CAP CERAFTI	601205-0221	CK12BX221K	81349
C38	220 PF 100V 10 CAP CERAFTI	601205-0221	CK12BX221K	81349
C39	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C40	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C41	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C42	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C43	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C44	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C45	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C46	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C47	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C48	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C49	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C50	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C51	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C52	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C53	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C54	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C55	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C56	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C57	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C58	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C59	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C60	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C61	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C62	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C63	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C64	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C65	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C66	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349

ASSEMBLY PCB Assy 1 MHZ PHASE SHIFTER (CONT)
ASSEMBLY NUMBER 10398083
REFERENCE DESIGNATOR PREFIX 1A1A2A4
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C67	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C68	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C69	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C70	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C71	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C72	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C73	150 PF 500V 5 CAP DIP MICA	603000-0151	DM15-151J	02799
C74	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C75	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
CR1	PRV75 DIO S STG	7011N914	1N914	81349
CR2	PRV75 DIO S STG	7011N914	1N914	81349
CR3	PRV75 DIO S STG	7011N914	1N914	81349
R1	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R2	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R3	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R4	100 K 1/4W 10 RES FXD COMP	651102-0104	RC07GF104K	81349
R5	12 K 1/4W 10 RES FXD COMP	651102-0123	RC07GF123K	81349
R6	12 K 1/4W 10 RES FXD COMP	651102-0123	RC07GF123K	81349
R7	100 K 1/4W 10 RES FXD COMP	651102-0104	RC07GF104K	81349
R8	5 K 1/2W 10 RES VAR CERMET	659011-0502	66XR5K	73138
R9	20.5K 1/8W 1 RES FXD FILM	653001-2052	RN55D2052F	81349
R10	12.1K 1/8W 1 RES FXD FILM	653001-1212	RN55D1212F	81349
R11	4.12K 1/8W 1 RES FXD FILM	653001-4121	RN55D4121F	81349
R12	20 K 1/8W 1 RES FXD FILM	653001-2002	RN55D2002F	81349
R13	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R14	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R15	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R16	9.09K 1/8W 1 RES FXD FILM	653001-9091	RN55D9091F	81349
R17	750 OHM 1/8W 1 RES FXD FILM	653001-7500	RN55D7500F	81349
R18	82.5K 1/8W 1 RES FXD FILM	653001-8252	RN55D8252F	81349
R19	20 K 1/2W 10 RES VAR CERMET	659011-0203	66XR20K	73138
R20	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R21	20 K 1/8W 1 RES FXD FILM	653001-2002	RN55D2002F	81349

ASSEMBLY PCB ASSY 1 MHZ PHASE SHIFTER (CONT)
ASSEMBLY NUMBER 10398083
REFERENCE DESIGNATOR PREFIX 1A1A2A4
QUANTITY FA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R22	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R23	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R24	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R25	9.09K 1/8W 1 RES FXD FILM	653001-9091	RN55D9091F	81349
R26	750 OHM 1/8W 1 RES FXD FILM	653001-7500	RN55D7500F	81349
R27	5 K 1/2W 10 RES VAR CERMET	659011-0502	66XR5K	73138
R28	16.2K 1/8W 1 RES FXD FILM	653001-1622	RN55D1622F	81349
R29	9.09K 1/8W 1 RES FXD FILM	653001-9091	RN55D9091F	81349
R30	10 OHM 1/4W 10 RES FXD COMP	651102-0100	RC07GF100K	81349
R31	82.5K 1/8W 1 RES FXD FILM	653001-8252	RN55D8252F	81349
R32	20 K 1/2W 10 RES VAR CERMET	659011-0203	66XR20K	73138
R33	NOT USED			
R34	20 K 1/8W 1 RES FXD FILM	653001-2002	RN55D2002F	81349
R35	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R36	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R37	10 K 1/8W 1 RES FXD FILM	653001-1002	RN55D1002F	81349
R38	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R39	9.09K 1/8W 1 RES FXD FILM	653001-9091	RN55D9091F	81349
R40	750 OHM 1/8W 1 RES FXD FILM	653001-7500	RN55D7500F	81349
R41	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
R42	2.2 K 1/4W 10 RES FXD COMP	651102-0222	RC07GF222K	81349
R43	330 OHM 1/4W 10 RES FXD COMP	651102-0331	RC07GF331K	81349
R44	10 OHM 1/4W 10 RES FXD COMP	651102-0100	RC07GF100K	81349
R45	NOT USED			
R46	2 K 1/2W 10 RES VAR CERMET	659011-0202	66XR2K	73138
R47	12.1K 1/8W 1 RES FXD FILM	653001-1212	RN55D1212F	81349
U1	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U2	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U3	IC ONESHOT DUAL	703SN74LS123	SN74LS123N	01295
U4	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U5	IC DUAL DECADE COUNTER	703SN74LS390	SN74LS390N	01295
U6	IC DUAL 4-BIT BINARY COUNTER	703SN74LS393	SN74LS393N	01295
U7	IC DUAL CASCADABLE 8-BIT COMPARATOR	70325LS2521	25LS2521	99547

ASSEMBLY PCB ASSY 1 MHZ PHASE SHIFTER (CONT)
ASSEMBLY NUMBER 10398083
REFERENCE DESIGNATOR PREFIX 1A1A2A4
QUANTITY FA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U8	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U9	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U10	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U11	IC QUADR 2-INP EXCL-OR GATES	703SN7486N	SN7486N	01295
U12	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U13	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U14	IC DUAL DECADE COUNTER	703SN74LS390	SN74LS390N	01295
U15	IC DUAL 4-BIT BINARY COUNTER	703SN74LS393	SN74LS393N	01295
U16	IC DUAL CASCADABLE 8-BIT COMPARATOR	70325LS2521	25LS2521	99547
U17	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U18	IC 8-BIT UP-COMPATIBLE D/A CONV	703NE5019N	NE5019N	18324
U19	IC GENERAL PURPOSE OP AMP	703MC1741CP1	MC1741CP1	04713
U20	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U21	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U22	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U23	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U24	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U25	IC DUAL DECADE COUNTER	703SN74LS390	SN74LS390N	01295
U26	IC DUAL 4-BIT BINARY COUNTER	703SN74LS393	SN74LS393N	01295
U27	IC DUAL CASCADABLE 8-BIT COMPARATOR	70325LS2521	25LS2521	99547
U28	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U29	IC 8-BIT UP-COMPATIBLE D/A CONV	703NE5019N	NE5019N	18324
U30	IC GENERAL PURPOSE OP AMP	703MC1741CP1	MC1741CP1	04713
U31	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U32	IC TRIPLE 3-INP NAND GATE	703SN74LS10N	SN74LS10N	01295
U33	IC PHASE LOCKED LOOP	703NE564N	NE564N	18324
U34	IC DUAL DECADE COUNTER	703SN74LS390	SN74LS390N	01295
U35	IC QUADR 2-INP NAND GATE	703SN74S00N	SN74S00N	01295
U36	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U37	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U38	IC QUADR TWO INPUT OR GATE	703SN74LS32N	SN74LS32N	01295
U39	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U40	IC 4-LINE TO 16-LINE DECODERS/MUX	703SN74154N	SN74154N	01295

ASSEMBLY PCB ASSY 1 MHZ PHASE SHIFTER (CONT)
ASSEMBLY NUMBER 10398083
REFERENCE DESIGNATOR PREFIX 1A1A2A4
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U41	IC SAMPLE AND HOLD GATED OP AMP	703HA-2425	HA1-2425-5	34371
U42	IC GENERAL PURPOSE OP AMP	703MC1741CP1	MC1741CP1	04713

ASSEMBLY PCB ASSY ACQUIRE/TRACK
ASSEMBLY NUMBER 10398087
REFERENCE DESIGNATOR PREFIX 1A1A2A5
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	330 UF 6 V 10 CAP TANT	608013-0337	CS13BB337K	81349
C2	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C3	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C4	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C5	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C6	150 PF 500V 5 CAP DIP MICA	603000-0151	DM15-151J	02799
C7	.001 UF 100V 20 CAP CERAFTI	601205-0102	CK12BX102M	81349
C8	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C9	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C10	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C11	1 UF 35V 10 CAP TANT	608017-0105	CS13BF105K	81349
C12	1 UF 35V 10 CAP TANT	608017-0105	CS13BF105K	81349
C13	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C14	1 UF 35V 10 CAP TANT	608017-0105	CS13BF105K	81349
C15	100 UF 20 V 10 CAP TANT	608016-0107	CS13BF107K	81349
C16	100 UF 20 V 10 CAP TANT	608016-0107	CS13BF107K	81349
C17	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C18	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BB104K	81349
C19	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C20	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C21	47 PF 500V 5 CAP DIP MICA	603000-0470	DM15-470J	02799
C22	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C23	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C24	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C25	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C26	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C27	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C28	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C29	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C30	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C31	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C32	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C33	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349

ASSEMBLY PCB ASSY ACQUIRE/TRACK (CONT)
ASSEMBLY NUMBER 10398087
REFERENCE DESIGNATOR PREFIX 1A1A2A5
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C34	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C35	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C36	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C37	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C38	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C39	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C40	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C41	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C42	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C43	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C44	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C45	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C46	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C47	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C48	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C49	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C50	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C51	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C52	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C53	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C54	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C55	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C56	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C57	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C58	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C59	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C60	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C61	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C62	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C63	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C64	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C65	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C66	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349

ASSEMBLY PCB ASSY ACQUIRE/TRACK (CONT)
ASSEMBLY NUMBER 10398087
REFERENCE DESIGNATOR PREFIX 1A1A2A5
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R1	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R2	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R3	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R4	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R5	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R6	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R7	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R8	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R9	4.87K 1/8W 1 RES FXD FTLM	653001-4871	RN55D4871F	81349
R10	11 K 1/8W 1 RES FXD FTLM	653001-1102	RN55D1102F	81349
R11	750 OHM 1/8W 1 RES FXD FTLM	653001-7500	RN55D7500F	81349
R12	1.1 K 1/8W 1 RES FXD FTLM	653001-1101	RN55D1101F	81349
R13	2 K 1/8W 1 RES FXD FTLM	653001-2001	RN55D2001F	81349
R14	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R15	10 K 1/8W 1 RES FXD FTLM	653001-1002	RN55D1002F	81349
R16	20 K 1/8W 1 RES FXD FTLM	653001-2002	RN55D2002F	81349
R17	10 K 1/8W 1 RES FXD FTLM	653001-1002	RN55D1002F	81349
R18	10 K 1/8W 1 RES FXD FTLM	653001-1002	RN55D1002F	81349
R19	10 K 1/8W 1 RES FXD FTLM	653001-1002	RN55D1002F	81349
R20	82.5K 1/8W 1 RES FXD FTLM	653001-8252	RN55D8252F	81349
R21	20 K 1/2W 10 RES VAR CERMET	659011-0203	66XR20K	73138
U1	IC QUADR TWO INPUT OR GATE	703SN74LS32N	SN74LS32N	01295
U2	IC 8-INP NAND GATE	703SN74LS30N	SN74LS30N	01295
U3	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U4	IC QUADR 2-INP EXCL-OR GATES	703SN74LS86N	SN74LS86N	01295
U5	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U6	IC QUAD 2-TO 1-LINE DATA SEL/MUX	703SN74158N	SN74158N	01295
U7	IC DUAL DECADE COUNTER	703SN74LS390	SN74LS390N	01295
U8	IC DUAL DECADE COUNTER	703SN74LS390	SN74LS390N	01295
U9	IC DUAL 4-BIT BINARY COUNTER	703SN74393N	SN74393N	01295
U10	IC TRIPLE 3-INP NAND GATE	703SN74LS10N	SN74LS10N	01295
U11	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U12	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295

ASSEMBLY PCB ASSY ACQUIRE/TRACK (CONT)
ASSEMBLY NUMBER 10398087
REFERENCE DESIGNATOR PREFIX 1A1A2A5
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U13	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U14	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U15	IC CMOS DUAL D-TYPE FLIP-FLOP	703MM74C74N	MM74C74N	40948
U16	IC CMOS DUAL D-TYPE FLIP-FLOP	703MM74C74N	MM74C74N	40948
U17	IC CMOS DUAL D-TYPE FLIP-FLOP	703MM74C74N	MM74C74N	40948
U18	IC DUAL D-TYPE FLIP FLOPS	703SN74L74N	SN74L74N	01295
U19	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U20	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U21	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U22	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U23	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U24	IC DUAL 4-BIT BINARY COUNTER	703SN74393N	SN74393N	01295
U25	8 BIT PARALLELOUT SER SHIFT REGUE	703SN74LS164	SN74LS164N	01295
U26	8 BIT PARALLELOUT SER SHIFT REGUE	703SN74LS164	SN74LS164N	01295
U27	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U28	IC 8-BIT UP-COMPATIBLE D/A CONV	703NE5019N	NE5019N	18324
U29	IC OCTAL INV BUFFER LINE DRVR/RCVR	703SN74LS240	SN74LS240N	01295
U30	IC OCTAL INV BUFFER LINE DRVR/RCVR	703SN74LS240	SN74LS240N	01295
U31	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U32	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U33	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U34	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U35	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U36	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U37	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U38	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U39	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U40	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U41	IC 8-BIT UP-COMPATIBLE D/A CONV	703NE5019N	NE5019N	18324
U42	IC OP AMP INTL COMPEN GEN PURPOSE	703MC1741CG	MC1741CG	04713
U43	IC 12 BIT D/A CONVERTER	703DAC80ZCBI	AD-DAC80Z-CBI-V	24355
U44	IC DUAL 4-BIT BINARY COUNTER	703SN74393N	SN74393N	01295
U45	IC DUAL CASCADABLE 8-BIT COMPARATOR	70325LS2521	25LS2521	99547

ASSEMBLY PCB ASSY ACQUIRE/TRACK (CONT)
ASSEMBLY NUMBER 10398087
REFERENCE DESIGNATOR PREFIX 1A1A2A5
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U46	IC DUAL CASCADABLE 8-BIT COMPARATOR	70325LS2521	25LS2521	99547
U47	IC DUAL 4-BIT BINARY COUNTER	703SN74393N	SN74393N	01295
U48	IC 4-LINE TO 16-LINE DECODERS/MUX	703SN74154N	SN74154N	01295
U49	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295

ASSEMBLY PCB ASSY MPU/MEMORY
ASSEMBLY NUMBER 10398079
REFERENCE DESIGNATOR PREFIX 1A1A2A6
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C2	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C3	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C4	22 PF 500V 5 CAP DIP MICA	603000-0220	DM15-220J	02799
C5	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C6	27 PF 500V 5 CAP DIP MICA	603000-0270	DM15-270J	02799
C7	27 PF 500V 5 CAP DIP MICA	603000-0270	DM15-270J	02799
C8	1 UF 35V 10 CAP TANT	608017-0105	CS13BF105K	81349
C9	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C10	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C11	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C12	56 PF 500V 5 CAP DIP MICA	603000-0560	DM15-560J	72136
C13	75 PF 500V 5 CAP DIP MICA	603000-0750	DM15-750J	72136
C14	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C15	.001 UF 250V 10 CAP POLYCARBONATE	610008-0102	B32540C/.001/10/250	25088
C16	220 PF 500V 5 CAP DIP MICA	603000-0221	CM05FD221J03	09023
C17	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C18	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C19	820 PF 300V 5 CAP DIP MICA	603000-0821	DM15-821J	72136
C20	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C21	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C22	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C23	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C24	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C25	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C26	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C27	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C28	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C29	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C30	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C31	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C32	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C33	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349

ASSEMBLY PCB ASSY MPU/MEMORY (CONT)
ASSEMBLY NUMBER 10398079
REFERENCE DESIGNATOR PREFIX 1A1A2A6
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C34	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C35	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C36	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C37	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C38	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C39	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C40	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C41	100 UF 20 V 10 CAP TANT	608016-0107	CS13BF107K	81349
C42	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C43	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C44	.1 UF 50 V 20 CAP CERAMTC	601100-0104	CY20C104M	71590
C45	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C46	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C47	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C48	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C49	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C50	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C51	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C52	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C53	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C54	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C55	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C56	.01 UF 100V 10 CAP CERAFTI	601205-0103	CK12BX103K	81349
C57	100 UF 20 V 10 CAP TANT	608016-0107	CS13BF107K	81349
C58	330 UF 6 V 10 CAP TANT	608013-0337	CS13BB337K	81349
CR1	PRV75 DIO S STG	7011N914	1N914	81349
CR2	NOT USED			
Q1	0.50W TO-92 XSTR NPNS SH	702MPS3646	MPS3646	04713
Q2	0.50W TO-92 XSTR NPNS SH	702MPS3646	MPS3646	04713
Q3	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
R1	470 OHM 1/4W 10 RES FXD COMP	651102-0471	RC07GF471K	81349
R2	5 K 1/2W 10 RES VAR CERMET	659011-0502	66XR5K	73138
R3	47 K 1/4W 10 RES FXD COMP	651102-0473	RC07GF473K	81349

ASSEMBLY PCB ASSY MPU/MEMORY (CONT)
ASSEMBLY NUMBER 10398079
REFERENCE DESIGNATOR PREFIX 1A1A2A6
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R4	8.66K 1/8W 1 RES FXD FILM	653001-8661	RN55D8661F	81349
R5	22 K 1/4W 10 RES FXD COMP	651102-0223	RC07GF223K	81349
R6	47 OHM 1/4W 10 RES FXD COMP	651102-0470	RC07GF470K	81349
R7	20 K 1/2W 10 RES VAR CERMET	659011-0203	66XR20K	73138
R8	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R9	2.2 K 1/4W 10 RES FXD COMP	651102-0222	RC07GF222K	81349
R10	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R11	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R12	47 K 1/4W 10 RES FXD COMP	651102-0473	RC07GF473K	81349
R13	5 K 1/2W 10 RES VAR CERMET	659011-0502	66XR5K	73138
R14	5 K 1/2W 10 RES VAR CERMET	659011-0502	66XR5K	73138
R15	3.92K 1/8W 1 RES FXD FILM	653001-3921	RN55D3921F	81349
R16	7.5 K 1/8W 1 RES FXD FILM	653001-7501	RN55D7501F	81349
R17	22.1K 1/8W 1 RES FXD FILM	653001-2212	RN55D2212F	81349
R18	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
R19	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
R20	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R21	10 K 1/4W 10 RES FXD COMP	651102-0103	RC07GF103K	81349
R22	56 OHM 1/4W 10 RES FXD COMP	651102-0560	RC07GF560K	81349
S1	SWITCH ROCKER SPDTX4 DIP	553012-0020	76C04	81073
S2	SWITCH, TOGGLE, ON-ON-ON PCB RA	553010-0026	TT21PAG-RA-9T1/4	95146
U1	IC LOW NOISE OP AMP	703NE5534AN	NE5534AN	18324
U2	IC TRIPLE 3-INP NAND GATE	703SN74LS10N	SN74LS10N	01295
U3	IC CMOS MICROPROCESSOR W/CLOCK/RAM	703MC6802P	MC6802P	04173
U4	IC OCTAL, BUFFER LINE DRVR/RCVR	703SN74LS244	SN74LS244N	01295
U5	IC OCTAL, INV BUFFER LINE DRVR/RCVR	703SN74LS240	SN74LS240N	01295
U6	IC 8-INP NAND GATE	703SN74LS30N	SN74LS30N	01295
U7	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295
U8	IC DUAL DECADE COUNTER	703SN74LS390	SN74LS390N	01295
U9	IC SAMPLE AND HOLD GATED OP AMP	703HA-2425	HA1-2425-5	34371
U10	IC SAMPLE AND HOLD GATED OP AMP	703HA-2425	HA1-2425-5	34371
U11	IC DUAL 2-TO-4 LINE DECODERS	703SN74LS139	SN74LS139N	01295
U12	IC 3 TO 8 LINE DECODER-MULTIPLEXER	703SN74LS138	SN74LS138N	01295

ASSEMBLY PCB ASSY MPU/MEMORY (CONT)
ASSEMBLY NUMBER 10398079
REFERENCE DESIGNATOR PREFIX 1A1A2A6
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U13	IC 8-INP NAND GATE	703SN74LS30N	SN74LS30N	01295
U14	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U15	IC QUADR TWO INPUT OR GATE	703SN74LS32N	SN74LS32N	01295
U16	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U17	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U18	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U19	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U20	IC DUAL 4-BIT BINARY COUNTER	703SN74LS393	SN74LS393N	01295
U21	IC DUAL 4-BIT BINARY COUNTER	703SN74LS393	SN74LS393N	01295
U22	IC DUAL 4-BIT BINARY COUNTER	703SN74LS393	SN74LS393N	01295
U23	IC DUAL 2-TO-4 LINE DECODERS	703SN74LS139	SN74LS139N	01295
U24	IC 8-INP NAND GATE	703SN74LS30N	SN74LS30N	01295
U25	IC OCTAL BUFFER LINE DRVR/RCVR	703SN74LS244	SN74LS244N	01295
U26	IC RAM 1KX4 BIT 200 NS CYCLE	703P2114A4	P2114A-4	34649
U27	IC RAM 1KX4 BIT 200 NS CYCLE	703P2114A4	P2114A-4	34649
U28	IC RAM 1KX4 BIT 200 NS CYCLE	703P2114A4	P2114A-4	34649
U29	IC RAM 1KX4 BIT 200 NS CYCLE	703P2114A4	P2114A-4	34649
U30	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U31	IC DUAL D-TYPE FLIP-FLOP	703SN74LS74N	SN74LS74N	01295
U32	IC 8-BIT A/D CONV. MPU COMPATIBLE	703AD570JD	AD570JD	24355
U33	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U34	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U35	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U36	IC OCTAL D-TYPE FF W/TSC AND CLOCK	703SN74LS374	SN74LS374N	01295
U37	IC OCTAL 3-STATE TRANSCEIVER	703SN74LS245	SN74LS245N	01295
U38	IC OCTAL 3-STATE TRANSCEIVER	703SN74LS245	SN74LS245N	01295
U39	10 K 1.5W 5 RES EXD SIPNET	654011-0103	750-101-R10K	23223
U40	IC OCTAL 3-STATE TRANSCEIVER	703SN74LS245	SN74LS245N	01295
U41	D2732 W/PROG P2100T CHIP 0	76006-2100T0		24672
U42	D2732 W/PROG P2100T CHIP 1	76006-2100T1		24672
U43	D2732 W/PROG P2100T CHIP 2	76006-2100T2		24672
U44	NOT USED			
U45	IC DUAL MONOSTABLE MULTIVIBRATOR	703SN74LS221	SN74LS221N	01295

ASSEMBLY PCB ASSY MPU/MEMORY (CONT)
ASSEMBLY NUMBER 10398079
REFERENCE DESIGNATOR PREFIX 1A1A2A6
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
W1	CABL, 26 CON X 3.0 IN.PCB MTG-HEAD	12096273-3		24672
XU1	REF DES XU1 THRU XU40 NOT USED			
XU41	SOCKET IC 24 PIN DIP, CLOSED ENT	551016-0004	IC-624-SGT	55322
XU42	SOCKET IC 24 PIN DIP, CLOSED ENT	551016-0004	IC-624-SGT	55322
XU43	SOCKET IC 24 PIN DIP, CLOSED ENT	551016-0004	IC-624-SGT	55322
XU44	NOT USED			
Y1	XTAL, 4.000000 MHZ	752A4000000	SCM18	27073

ASSEMBLY PCB ASSY +5 VOLT REGULATOR
ASSEMBLY NUMBER 10398059
REFERENCE DESIGNATOR PREFIX 1A1A2A7
QUANTITY FA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	100 UF 50V 10 CAP ELEC MTN	602039-0035	39D107G050EJ4	56289
C2	0.1 UF 50 V 10 CAP CERIFTI	601205-0104	CK14BR104K	81349
C3	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C4	220 PF 500V 5 CAP DIP MICA	603000-0221	CM05FD221J03	09023
C5	.01 UF 100V 10 CAP CERAMIC	601105-0103	CN40A103K	71590
C6	2000 UF 15 V CAP ELECTROLYTIC	602000-0013	TC1520C	90201
C7	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
CR1	PRV75 DIO S STG	7011N914	1N914	81349
CR2	40V 25 AMP DIO S	7011N5831	1N5831	04713
P1	EDGE CONNECTOR			
P2	CONN 10PIN MALE VERTICAL	551107-6610	87215-2	74868
L1	281 UH INDUCTOR POWER	751110-5455	5455	00000
Q1	TSTR POW DARLINGTON 12A	7022N6051	2N6051	41282
R1	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R2	1 K 1/2W 10 RES VAR CERMET	659018-0102	850W-1K	65092
R3	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R4	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R5	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R6	100 K 1/4W 10 RES FXD COMP	651102-0104	RC07GF104K	81349
R7	23.7K 1/8W 1 RES FXD FILM	653001-2372	RN55D2372F	81349
R8	1 K 3 W 5 RES FXD W.W.	652242-0102	242E-1025	56289
R9	6.65K 1/8W 1 RES FXD FILM	653001-6651	RN55D6651F	81349
R10	150 OHM 1/4W 10 RES FXD COMP	651102-0151	RC07GF151K	81349
U1	IC SWITCH MODE REG CONTROLLER	703SG3524J	SG3524J	34333
U2	POWER SUPPLY EL-TYPE 5V IN=65V OUT	570902-0001	0616	32890
U3	IC OVP, 5V SUPPLIES (6.6V TRIP)	703L60V-5	L-6-0V-5	80103

ASSEMBLY OPT 01 IEEE-488(GPIB) INTERFACE
ASSEMBLY NUMBER 12898484
REFERENCE DESIGNATOR PREFIX 1A1A3
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	PCB ASSY GENL PURP INTERFACE BUS	10398250		24672
W1	CABLE ASSY 26 CONDUCTOR	12098095		24672

ASSEMBLY PCB ASSY GENL PURP INTERFACE BUS
ASSEMBLY NUMBER 10398250
REFERENCE DESIGNATOR PREFIX 1A1A3A1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C2	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C3	330 UF 6 V 10 CAP TANT	608013-0337	CS13BB337K	81349
C4	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
C5	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
P1	CONN 24 POSITION RIGHT ANGLE PCB	551026-0650	552791-1	04618
P2	CONN 26 PIN	551107-6626	87215-9	00779
R1	10 K 1.5W 5 RES FXD SIPNET	654011-0103	750-101-R10K	23223
R2	3.3 K 1/4W 10 RES FXD COMP	651102-0332	RC07GF332K	81349
S1	SWITCH, ROCKER SPST 76B08	553012-0010	76B08	81073
U1	IC DUAL 4-INP NAND GATE	703SN74LS20N	SN74LS20N	01295
U2	IC NMOS GENERAL INTERFACE ADAPTER	703MC68488P	MC68488P	04173
U3	IC OCTAL BI-DIRECTIONAL TRAN-REC	703MC3447P	MC3447P	04173
U4	IC OCTAL 3-STATE TRANSCEIVER	703SN74LS245	SN74LS245N	01295
U5	IC OCTAL BI-DIRECTIONAL TRAN-REC	703MC3447P	MC3447P	04173
U6	IC QUADR 2-INP NAND GATE	703SN74LS00N	SN74LS00N	01295
U7	IC OCTAL, BUFFER LINE DRVR/RCVR	703SN74LS244	SN74LS244N	01295
XS1	IC 16 PIN SOCKET RT ANGLE MTG.	551015-9997	516-AG7D	91506

ASSEMBLY PANEL ASSY REAR
ASSEMBLY NUMBER 10998047
REFERENCE DESIGNATOR PREFIX 1A1A4
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
J1	CONN, FEMALE BNC ISOLATED FRM PANEL	551100-0010	31-010	74868
J2	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J3	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J4	CONN, FEMALE BNC ISOLATED FRM PANEL	551100-0010	31-010	74868
J5	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J6	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J7	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J8	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J9	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J10	CONN, FEMALE BNC STANDARD TYPE	551100-0625	UG-625B 31-236	74868
J11	POST,RED BINDING	551110-0002	111-0102-001	74970
J12	POST,BLK BINDING	551110-0000	111-0103-001	74970
J13	POST,RED BINDING	551110-0002	111-0102-001	74970
J14	POST,BLK BINDING	551110-0000	111-0103-001	74970
J15	CONN, BOX MOUNT 3-PIN CONTACT	551102-0016	MS3102A-14S-1P	96906
J16	FILTER LINE 6AMP 115-230V 50-60HZ	799005-0002	6EF2	05245
S1	SWITCH, TOGGLE, DPDT	553010-0006	MST-205N	95146
S2	SWITCH, DPDT 115/230V SLIDE	553007-0001	46256LFR	82389
XF1	HOLDER,FUSE	507003-2012	342012	75915
XF2	HOLDER,FUSE	507003-2012	342012	75915

AUSTRON INC. 1915 KRAMER LANE, AUSTIN, TEXAS 78758 (512) 836-3523 TWX 910/874-1356

AUSTRON INC

MANUAL PARTS LIST MODEL 2100 23 MAR 82

ASSEMBLY PCB ASSY INPUT/OUTPUT BUFFERS
ASSEMBLY NUMBER 10399019
REFERENCE DESIGNATOR PREFIX DATA
QUANTITY 001 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	330 UF 6 V 10 CAP TANT	608013-0337	CSR13B337K	81349
C2	.1 UF 50 V 20 CAP CERAMIC	601100-0104	CY20C104M	71590
CR1	PRV75 DIO S SIG	7011N914	1N914	81349
CR2	PRV75 DIO S SIG	7011N914	1N914	81349
Q1	0.50W TO-92 XSTR NPNS SH	702MPS3646	MPS3646	04713
Q2	0.50W TO-92 XSTR NPNS SH	702MPS3646	MPS3646	04713
Q3	0.50W TO-92 XSTR NPNS SH	702MPS3646	MPS3646	04713
Q4	0.50W TO-92 XSTR NPNS SH	702MPS3646	MPS3646	04713
Q5	0.50W TO-92 XSTR NPNS SH	702MPS3646	MPS3646	04713
R1	2.2 K 1/4W 10 RES FXD COMP	651102-0222	RC07GF222K	81349
R2	4.7 K 1/4W 10 RES FXD COMP	651102-0472	RC07GF472K	81349
R3	22 K 1/4W 10 RES FXD COMP	651102-0223	RC07GF223K	81349
R4	470 OHM 1/4W 10 RES FXD COMP	651102-0471	RC07GF471K	81349
R5	56 OHM 1/4W 10 RES FXD COMP	651102-0560	RC07GF560K	81349
R6	47 OHM 1/4W 10 RES FXD COMP	651102-0470	RC07GF470K	81349
R7	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
R8	1.5 K 1/4W 10 RES FXD COMP	651102-0152	RC07GF152K	81349
R9	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
R10	150 OHM 1/4W 10 RES FXD COMP	651102-0151	RC07GF151K	81349
R10	150 OHM 1/4W 10 RES FXD COMP	651102-0151	RC07GF151K	81349
R11	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
R13	150 OHM 1/4W 10 RES FXD COMP	651102-0151	RC07GF151K	81349
R13	150 OHM 1/4W 10 RES FXD COMP	651102-0151	RC07GF151K	81349
R15	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
R16	2.2 K 1/4W 10 RES FXD COMP	651102-0222	RC07GF222K	81349
R1M	1 K 1/4W 10 RES FXD COMP	651102-0102	RC07GF102K	81349
U1	IC QUAD, 50-OHM LINE DRIVER	703SN74128N	SN74128N	01295
U2	IC DUAL LINE DRIVER	703N8T23	N8T23	18324
U3	IC DUAL LINE DRIVER	703N8T23	N8T23	18324

APPENDIX

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INTRODUCTION

Loran-C is a complex hyperbolic radio-navigation system developed by skilled engineers and maintained by highly-trained electronic technicians of the United States Coast Guard. LORAN stands for LOng RAnge Navigation. It is an electronic system using several cesium beam frequency standards as its time and frequency reference sources and Coordinated Universal Time (UTC) as its time scale. It is a network system using land-based transmitters which are closely monitored by the United States Naval Observatory (USNO), as well as the United States Coast Guard.

The Loran-C network is made up of several CHAINS. Three or more transmitting stations form a Loran-C chain. One transmitting station is designated MASTER (M), while the other stations are designated SECONDARY, i.e., Whiskey (W), Xray (X), Yankee (Y), and Zulu (Z). Chain coverage is determined by the power transmitted from each station, the distance between them, and their orientation. All of the stations within a chain transmit groups of pulses at the same repetition rate and carrier frequency, but not simultaneously.

The times of transmission are controlled so that, no matter where a receiver is located within the groundwave coverage area, pulses from the master station will be received first, followed by pulse groups from each successive secondary station. This is accomplished by each secondary station being delayed a controlled amount, called the EMISSION DELAY, so that the MASTER is always received first and no possibility exists of receiving pulse groups in reverse order. These emission delays are also selected so that no two groups overlap within the receiving distance from the station. (Reference Table A-1 for Loran-C chain make-up).

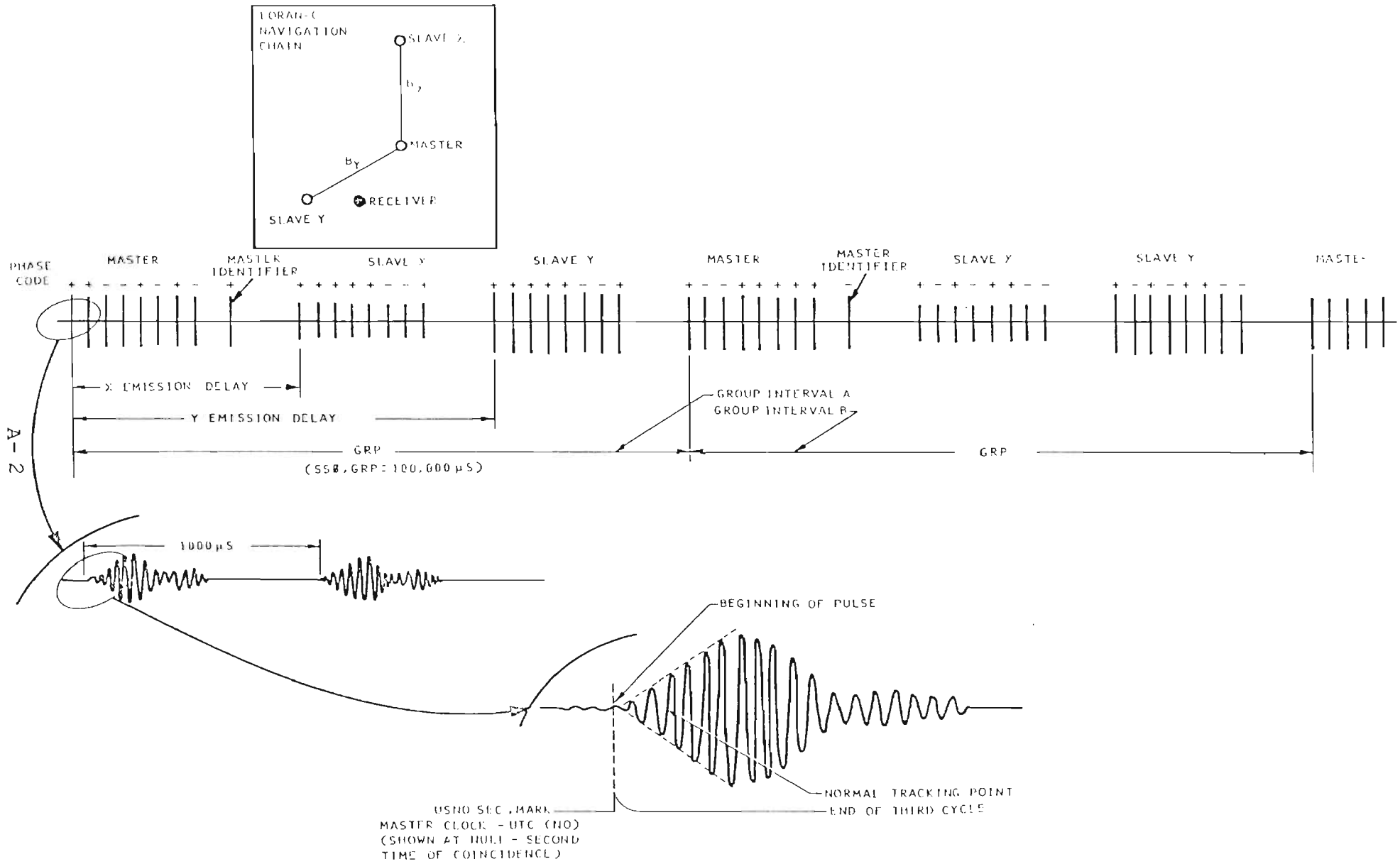

Figure A-1 Timing of Loran-C Signals

LORAN-C NETWORK

CHAIN	GRI	TRANSMITTER	COORDINATES	TED (μSEC)	PWR (KW)
Central Pacific	49900	M Johnston Is., HI	16 44 44.0 N 169 30 31.2 W		275
		X Upolu, PT., HI	20 14 49.2 N 155 53 09.7 W	15972.23	275
		Y Kure Is., HI	28 23 41.8 N 178 17 30.2 W	34253.17	275
Canadian East Coast	59300	M Caribou, ME	46 48 27.2 N 67 55 37.7 W		350
		X Nantucket, MA	41 15 11.9 N 69 58 39.1 W	13131.88	275
		Y Cape Race, NFLD	46 46 32.2 N 53 10 28.2 W	28755.02	1500
Sea of Japan (Commando Lion)*	59700	M Pohang, Korea	36 11 02.1 N 129 20 25.8 E		30
		W Hokkaido, Japan	42 44 37.1 N 143 43 09.2 E	15783.68	1000
		X Kwang Ju, Korea	35 02 27.5 N 126 32 31.4 E	31947.02	30
		Y Gesashi, Okinawa	26 36 25.0 N 128 08 56.4 E	45565.56	1000
Canadian West Coast	59900	M Williams Lake, BC	51 57 58.8 N 122 22 02.2 W		400
		X Shoal Cove, AK	55 26 20.9 N 131 15 19.7 W	13343.60	540
		Y George, WA	47 03 48.0 N 119 44 39.5 W	28927.36	1600
		Z Port Hardy, BC	50 36 29.7 N 127 21 29.0 W	42266.63	400
North Atlantic	79300	M Angissoq Greenland	59 59 17.3 N 45 10 27.5 W		760
		W Sandur, Iceland	64 54 26.6 N 23 55 21.8 W	15068.03	1500
		X Ejde, Faeroe Is., Denmark	62 17 59.6 N 07 04 26.1 W	27803.77	325
		Z Cape Race, NFLD	46 46 32.2 N 53 10 28.2 W	48212.20	1500
Gulf of Alaska	79600	M Tok, AK	63 19 42.8 N 142 48 31.9 W		540
		X Narrow Cape, AK	57 26 20.2 N 152 22 11.3 W	13804.45	400
		Y Shoal Cove, AK	55 26 20.9 N 131 15 19.7 W	29651.14	540
Norwegian Sea	79700	M Ejde, Faeroe Is., Denmark	62 17 59.6 N 07 04 26.1 W		325
		W Sylt, Germany	54 48 29.9 N 08 17 36.3 E	30065.64	275
		X BO, Norway	68 38 06.2 N 14 27 47.0 E	15048.10	165
		Y Sandur, Iceland	64 54 26.6 N 23 55 21.8 W	48944.53	1500
		Z Jan Mayen, Norway	70 54 52.6 N 08 43 58.7 W	63216.30	165
Southeast U.S.	79800	M Malone, FL	30 59 38.7 N 85 10 09.3 W		800
		W Grangeville, LA	30 43 33.0 N 90 49 41.6 W	12809.54	800
		X Raymondville, TX	26 31 55.0 N 97 50 00.1 W	27443.38	400
		Y Jupiter, FL	27 01 58.5 N 80 06 53.5 W	45201.88	275
		Z Carolina Be., NC	34 03 46.0 N 77 54 46.8 W	61542.72	550
Mediterranean Sea	79900	M Sellia Marina, It	38 52 20.6 N 16 43 06.2 E		165
		X Lampedusa, It	35 31 20.8 N 12 31 30.3 E	12759.98	325
		Y Kargabarun, Turk.	40 58 21.0 N 27 52 01.5 E	32273.30	165
		Z Estartit, Spain	42 03 38.5 N 03 12 15.5 E	50999.71	165
Great Lakes	89700	M Dana, IN	39 51 07.5 N 87 29 12.1 W		400
		W Malone, FL	30 59 38.7 N 85 10 09.3 W	14355.11	800
		X Sencca, NY	42 42 50.6 N 76 49 33.9 W	31162.06	800
		Y Baudette, MN	48 36 49.8 N 94 33 18.5 W	47753.74	500
West Coast U.S.	99400	M Fallon, NV	39 33 06.6 N 118 49 56.4 W		400
		W George, WA	47 03 48.0 N 119 44 39.5 W	13796.90	1600
		X Middletown, CA	38 46 57.0 N 122 29 44.5 W	28094.50	400
		Y Searchlight, NV	35 19 18.2 N 114 48 17.4 W	41967.30	540
Northeast U.S.	99600	M Seneca, NY	42 42 50.6 N 76 49 33.9 W		800
		W Caribou, ME	46 48 27.2 N 67 55 37.7 W	13757.20	350
		X Nantucket, MA	41 15 11.9 N 69 58 39.1 W	26969.93	275
		Y Carolina Be., NC	34 03 46.0 N 77 54 46.8 W	42221.65	550
		Z Dana, IN	39 51 07.5 N 87 29 12.1 W	57162.06	400
Northwest Pacific	99700 **	M Iwo Jima, Japan	24 48 03.6 N 141 19 30.3 E		1800
		W Marcus Is., Japan	24 17 07.9 N 153 58 53.2 E	15283.94	1800
		X Hokkaido, Japan	42 44 37.1 N 143 43 09.3 E	36685.12	1000
		Y Gesashi, Japan	26 36 25.0 N 128 08 56.5 E	59463.18	1000
		Z Yap Island, USA	09 32 45.8 N 138 09 55.0 E	80746.79	1000
North Pacific	99900	M St. Paul, AK	57 09 12.3 N 170 15 06.8 W		275
		X Attu, AK	52 49 44.0 N 173 10 49.0 E	14875.25	275
		Y Pt. Clarence, AK	65 14 40.3 N 166 53 12.6 W	32068.95	1000
		Z Narrow Cape, AK	57 26 20.2 N 152 22 11.3 W	46590.45	400

CHAIN - The Loran-C transmitters and the basic chain configuration.
GRI - The Loran-C Group Repetition Interval (transmission rate) in microseconds.
TRANSMITTER - M = Master Transmitter of the Loran-C chain.
W-Z = Secondary Transmitter identification letter within a given chain.
COORDINATES - Location of transmitter antenna.
TED - Total emission delay. This is the sum of the coding delay and baseline length in microseconds.
PWR (KW) - Transmitter radiated power in kilowatts.
SOURCE - United States Coast Guard Specification of the Transmitted Loran-C Signal July 1981, COMDTINST M16562.4 (with the exception of Commando Lion).
* - Expected to be operational in 1981.
** - Chain reconfigures when M antenna is down for maintenance. This occurs approximately every 3-4 years for a 30-60 day period. Marcus Island becomes M and the GRI is temporarily changed to 79300. Last temporary reconfiguration was FEB 1981.

TABLE A-1

CHARACTERISTICS

Loran-C operates in the frequency spectrum of 90 to 110 KHz with a carrier frequency of 100 KHz (LF). The low frequency of 100 KHz was chosen for propagation stability and for low attenuation of the groundwave with distance. Thus, highly stable, long-range transmission is possible. Pulsed and phase coded signals are used to minimize the effects of skywave interference. Phase coding also aids in eliminating certain types of CW interference. All Loran-C stations transmit groups of eight phase coded pulses separated from each other in time, by one millisecond. The master station transmits an additional ninth pulse, called the master identifier, which is separated from the first eight pulses by two milliseconds. In between pulse groups, the stations are silent; no carrier wave is transmitted. (Reference Figure A-1).

Each Loran-C station operates with a specified Group Repetition Interval (GRI) and all stations within a chain operate with the same GRI. An interval begins with the transmission of the master pulse group, followed by the transmissions of the secondary pulse groups (reference Figure A-1 and Table A-1).

To reduce carrier wave and skywave interference, the phase of the 100KHz carrier is varied from pulse to pulse in the pulse group, as shown in Figure A-1. To simplify the notation, a "+" sign describes a pulse with $\overline{0}$ radian phase and a "-" sign describes a pulse with π radian phase. There are two different phase codes for the master and two different phase codes for the secondaries. During the first GRI of a frame (a frame consists of 2 successive GRIs), the Group Interval A phase codes for the master and secondaries are used. During the second GRI, the Group Interval B phase codes are used.

By agreement with the United States Naval Observatory (USNO) the first master pulse of Group Interval A is synchronized to the Universal Time Coordinated (UTC) second. Because the GRI's of chains differ, it is

necessary to relate the timing of all master stations to a common epoch. This epoch is 0 hr, 0 min, 0 sec, 1 January 1958.

The expected times-of-coincidence (TOC) of a master station's transmissions with the UTC second are published in the Times of Coincidence, Null Ephemeris Tables, Series 9 developed by and available from the U.S. Naval Observatory. The difference between the time of the master's transmission with respect to UTC is also published by USNO in the Series 4 Bulletin. USNO Time Service Information letter of 15 August 1973, provides guidelines for making time measurements.

BLINK TRANSMISSIONS

When a malfunction exists at one of the transmitters in a Loran-C chain which affects the navigation/timing accuracy of the transmitter, both the master and the ailing secondary stations will begin "BLINK" transmissions. The ninth pulse from the master station is turned on and off, in a predefined code, to indicate which stations are affected. The first eight pulses of the master are never blinked. If a secondary transmitter is malfunctioning, the first two of its eight pulses will be blinked. The duration of the "on" time will be between 0.20 and 0.35 seconds, repeated every four seconds. The remaining six pulses will remain "on" continuously with the normal phase codes.

The errors of each chain are known and this information is published by the USNO on a daily and weekly basis, and the National Bureau of Standards (NBS) on a monthly basis. The status of the Loran-C chains are also published by the USNO, NBS, and the U.S. Coast Guard. See Figure A-3 for reference material and instructions on how to acquire published Loran-C information reports from these sources.

UNIVERSAL TIME SCALES

Time is a measure of the period of rotation of the earth. Historically, the time scale is derived by observing the zenith passage of a given star through the observer's meridian. However, the irregular wobble of the

earth on its axis causes timing variations according to the observer's position on the earth which may amount to as much as 30 milliseconds. In addition to rotational axis instability, the seasonal variation in the rate of rotation of the earth, which turns faster in the spring and slower in the autumn can cause cumulative effects amounting to 30 milliseconds per day.

In discussing the time derived from the observations of the earth's rotational period, it is necessary to distinguish between three systems of Universal Time (UT): UT0 (which is not truly Universal since it differs from place to place on the surface of the earth) is the time observed by zenith passage of a given star through the observer's meridian. UT1 is UT0 corrected for the effects of polar axis variation and is, therefore, the same everywhere. UT2 is smoothed UT1 corrected for the seasonal variation in the rate of earth rotation.

All of the above forms of Universal Time are subject to irregular variations which are caused by unpredictable and long term variations in the rotation of the earth and, therefore, have proved unsuitable as the basis for the unit of time for high precision physical measurements.

To provide the uniform, reproducible time scale needed for physical measurements, the second was defined in terms of an atomic frequency, viz: the duration of 9,192,631,770 periods of the radiation corresponding to the transition between the two hyperfine levels of the ground state of the cesium 133 atom. A Universal Time Scale, based on the use of a cesium atomic frequency standard is now the basic universal timing standard. This coordinated Universal Time (UTC) is the uniform second time scale broadcast by WWV,WWVH, and to which Loran-C is also related.

LEAP SECONDS

Due to variations in the earth's movement about its axis, small differences between UTC and UT1 time scales accumulate. Beginning in January 1972, leap seconds were introduced into UTC time to keep

synchronism with UT1 to within ±0.7 seconds. These adjustments when required are made on the last day of a UTC month preferably December 31 and/or June 30.

LORAN-C PROPAGATION

When radio energy is transmitted, a portion of the radiated emission travels out from the antenna parallel to the surface of the earth. This is known as the "groundwave." Another portion of the radiated emission travels upward and outward, encounters the ionosphere and is reflected back to earth. Reflections from the ionosphere are known as "skywaves." Unlike the skywave, the groundwave amplitude and phase are not influenced by factors that depend on the time of day, season of the year, etc. Both groundwave and skywave signals are used for navigation, frequency calibration, and timing. Despite its stability, the groundwave is not useful at an unlimited range from the transmitter. Two factors are responsible for this: primarily, the attenuation of the groundwave is relatively high, and its range increases at ranges beyond roughly 1000 nautical miles, so that the groundwave signal finally becomes "buried" in noise and interference. Also, the delay from the arrival of the groundwave to the arrival of the skywaves, large at short ranges, finally diminishes to the point of allowing contamination of the much smaller groundwave by the skywave. These factors establish the "groundwave range" at approximately 1,500 nautical miles. In areas of high noise and CW interference, this range may be greatly reduced. Within groundwave range of the station, the highly stable groundwave pulse may be used for very precise navigation, timing, and frequency measurement. The groundwave is stable to within tens of nanoseconds and is unaffected by diurnal phase shifts and other phenomena caused by ionospheric disturbances which plague skywave reception and CW systems.

SKYWAVE CONTAMINATION

Receiving antennas respond to a vector summation of both the groundwave and skywave. Since the skywave travels through a greater distance than

the groundwave, the skywave reaches the receiving antenna at a later time than the groundwave. The exact time of arrival of the skywave depends both on the geographic location of the receiving antenna and the separation between the lower region of the ionosphere and the surface of the earth. This latter condition is subject to both periodic and random fluctuations. Phase records taken from the rear portion of a Loran-C pulse will generally show at least some degree of instability because of changes in ion concentration in the ionosphere, while the front portion of the pulse remains reasonably free of skywave contamination (except at very great distances from the transmitting antenna, where both the groundwave and the skywave travel nearly the same distances).

ATMOSPHERIC NOISE

All Loran-C transmissions are affected, to some degree, by atmospheric noise. The background noise level at any given geographic location is a complex function of propagation path and atmospheric noise. Under normal conditions, long receiver tracking time constants are usually enough to minimize the essentially random effects of the noise.

CARRIER WAVE INTERFERENCE

Carrier wave interference may be synchronous (if the interferring frequency occurs on one of the spectral lines of the Loran-C pulse) or non-synchronous (if the carrier wave frequency does not coincide with one of the spectral lines). A common method for reducing the magnitude of non-synchronous carrier wave interference involves the use of narrow bandwidth, adjustable frequency band-reject filters which are tuned to the interferring frequencies without appreciably affecting the Loran-C pulse spectrum.

USING LORAN-C FOR TIME AND FREQUENCY MANAGEMENT

Due to the timing accuracy required of the Loran-C chain for radio-navigation and the advancements made in radio frequency receivers, precise time and frequency management can be achieved with excellent results. This can be accomplished with very little operator time, and with average operator skill.

LORAN-C TIMING WORKSHEET

STATION DATA

(1) Location/Site_____Date_____

(2) Chain_____

(3) GRI_____μsec

(4) Station_____Lat_____Long_____

(5) Emission Delay_____μsec

(6) Receiver Model_____S/N_____

(7) Receiver Delay_____μsec

(8) Receiver Antenna Location_____Lat_____Long_____

(9) Propagation Distance_____N. M.

(10) Basic Propagation Delay_____μsec

TIME OF COINCIDENCE (TOC)

(1) First TOC of the Day_____UTC

TOTAL TIMING DELAY (T^2D) AND TIME ERROR COMPUTATION

(1) Emission Delay_____μsec

(2) Groundwave Delay_____μsec

(3) Skywave Correction_____(___HOPS)

(4) Total Receiver Delay_____μsec

(5) USNO Correction_____μsec

(6) T^2D (Calculated, total sum of 1-5)_____μsec

(7) T^2D (Measured)_____μsec

(8) Local Time Error (Difference Between 6-7)_____μsec

Figure A-2

TIME AND FREQUENCY SERVICE INFORMATION

Time and Frequency service information can be obtained from the following sources:

1) Loran-C Education and Information Project U.S. Coast Guard Headquarters (G-NRN/TP14), Washington, D.C. 20593.
   Telephone number 202/472-5857.
   Ask for: (a) To be placed on their mailing list for Loran-C.
   (b) Loran-C User Handbook COMDTINST M16562.3.

2) United States Naval Observatory, Time Services Division, 34 Massachusetts Avenue, Washington, D.C. 20390.
   Telephone number 202/254-4546, Autovon 294-4546, TWX 710-822-1790.
   Ask for: (a) Loran-C Time of Coincidence (NULL) Ephemeris. Time Service Announcement, Series 4,9, and 16.
   (b) To be placed on their mailing list for Loran-C chain data. (See pages 14a, 14b, and 14c.)
   (c) Qualified requestors may obtain station propagation delays from the USNO. Requests should be accompanied by receiving stations coordinates, and a list of Loran-C transmitters to be monitored.

3) Time and Frequency Division, National Measurement Laboratory, National Bureau of Standards, Boulder, Colorado 80303. Telephone number 303/497-3378. Ask to be placed on their mailing list for Time and Frequency bulletins. (See Page 14d.)

If you need any assistance, please call AUSTRON, INC., Customer Service Office, 1915 Kramer Lane, Austin, Texas 78758. Telephone number 512/836-3523.

Figure A-3

TIME SERVICE PUBLICATIONS

Superintendent
Naval Observatory
Attn: Time Service Division
Washington, D.C. 20390

Series 1 WORLDWIDE PRIMARY TIME and FREQUENCY VLF and HF TRANSMISSIONS. Includes call sign, geographic location, frequencies, radiated power, times of broadcast, etc., of radio transmissions suitable for precise time measurement. Contains sections pertaining to US Navy time and frequency transmissions, Loran-C and Loran-D, Omega, National Bureau of Standards (NBS) and other time signals. (Issued as necessary.)

Series 4 DAILY PHASE VALUES and TIME DIFFERENCES. Lists observed phase and/or time differences between VLF, LF, Omega, television, portable clock measurements, Loran-C stations and the U.S. Naval Observatory (USNO) master clock, UTC (USNO, MC). Propagation distrubances and notices of interest for precision timekeeping are also given. (Issued weekly.)

Series 5 USNO PHASE VALUES/TELETYPE MESSAGE. Lists information described in Series 4 as it becomes available. TWX message for U.S. Government addresses only. (Issued each work day.)

This information is also available via recorded message by calling (202) 254-4662 or Autovon 294-4662.

The requirement to receive the TWX MESSAGE must be established in writing to:

Superintendent
U.S. Naval Observatory
Attn: Time Service Division
Washington, D.C. 20390

Series 6 A.1 - UT1 DATA. Lists daily values of polar coordinates, correction for seasonal variation, and A.1 - UT1 as observed at USNO and Naval Observatory Time Service Substation (NOTSS), Richmond, Florida. The astronomical latitude as observed at each station is also given. (Issued monthly.)

This information is also available in machine-readable form at the usual exchange ratio of three-to-one.

Series 7 PRELIMINARY TIMES and COORDINATES of the POLE. Lists general time scale information, values of UT1-UTC predicted two weeks in advance, the Bureau International de l'Heure (BIH) Rapid Service values of UT1-UTC and polar coordinates. (Issued weekly.)

Series 8 TIMES of COINCIDENCE (NULL) EPHEMERIS TABLES for TELEVISION. At present these tables are applicable only for WTTG Washington, D.C. They may be of interest in countries operating on the NTSC system. (Issued annually.)

Series 9 TIMES of COINCIDENCE (NULL) EPHEMERIS TABLES for LORAN. Individual tables are issued for the master station of each Loran-C chain and the master station of the Loran-D chain.

Series 10 ASTRONOMICAL PROGRAMS. Includes information pertaining to results, catalogs, papers, etc., concerning the Photographic Zenith Tube (PZT), Danjon Astrolabe, and Dual-Rate Moon Position Camera. (Issued as available.)

Frequently this information will be released as a Time Service Announcement Series 14.

Series 11 TIME SERVICE REPORT. Lists general timing information and time differences between coordinated stations and the UTC time system; adopted differences UT1-UTC and A.1 - UT1; UTC (USNO, MEAN) - UTC (USNO, MC); UTC (USNO, MC) - UTC (BIH); astronomical latitude and UT1 - UTC as observed at USNO and NOTSS: polar coordinates and corrections for seasonal and polar (longitude) variations. (Issued annually.)

Series 13 PRECISE TIME and TIME INTERVAL PLANNING MEETING. Includes announcement of the meeting held each December in Washington, D.C., the call for papers, and the preliminary program.

Series 14 TIME SERVICE ANNOUNCEMENTS. Includes general information petaining to time determination, measurement, and dissemination. (Issued as required.)

Series 15 BUREAU INTERNATIONAL de l'HEURE CIRCULAR D. Lists Universal Time and coordinates of the pole; emission time of time signals; Universal Time (Coordinated) from Loran-C and television pulse receptions and independent local atomic time scales (AT_i). This publication is distributed to U.S. addresses only. (Issued monthly.)

Series 16 PRECISE TIME TRANSFER REPORT. Lists the time difference UTC (USNO, MC) - UTC (reference clock), adjustments to reference clocks and portable clock measurements. The time difference is obtained via communication satellite time transfer, television and/or Loran-C receptions. (Issued each 20 days.)

Series 17 TRANSIT SATELLITE REPORT. Lists the difference UTC (satellite clock) - UTC (USNO, MC) and the frequency offset for each of the operational satellites. The information published is received from Naval Astronautics Group, Pt. Mugu, California. (Issued weekly.)

REQUEST FOR TIME SERVICE PUBLICATIONS

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19 November 1980

TIME SERVICE ANNOUNCEMENT, SERIES 9 NO. 175

1981 TIMES OF COINCIDENCE (NULL EPHEMERIS
GREAT LAKES USA (8970) LORAN-C
JANUARY-JUNE

Reference: (a) Time Service Information Letter of 15 Aug 1973
(b) Time Service Announcement, Series 14, No. 28

1. As stated in reference (b), the Bureau International de l'Heure (BIH) has announced that there will be NO STEP in the UTC Time Scale December 1980. Any introduction of a leap second in 1981 will be announced approximately 8 to 10 weeks in advance.

2. If a leap second is introduced, Times of Coincidence Table 1, incorporating that step, will be reissued. As Tables 2 and 3 remain valid, they will not be reissued and should be retained for future use. Beginning 1 January 1981, Table 3 will be issued only upon request.

3. The repetition rate of the 8970 chain is 89,700 microseconds and the beginning of the first pulse of one of the groups is emitted at a particular second on the UTC Time Scale. That pulse is synchronized to the U.S. Naval Observatory Master Clock (USNO MC).

4. The times of coincidence of the beginning of the reference pulse with USNO MC are found for each day by adding the values of Table 2 to the value of Table 1.

Assume that an operator monitoring a station of the above chain desires to make a synchronization check between the station clock and the Loran transmissions at about 1800 UT on 15 January.

From Table 2, the values near 1800 UT are:

H	M	S
17	41	27
17	56	24
18	11	21

These are added to the value from Table 1 listed for 15 January:

H	M	S
00	02	45

The times of coincidence between the beginning of the Loran reference pulse and the USNO MC one-pulse-per-second near the time of interest are then:

H	M	S
17	44	12
17	59	09
18	14	06

5. Between the times of coincidence as given by Tables 1 and 2, the time difference between any one-pulse-per-second of the USNO MC and the immediately following first (reference) pulse of a Loran group can be determined by using Table 3.

Assume that such a time difference is required at 17h 59m 59s on 15 January. From Tables 1 and 2, we found that the last null occurred at 17h 59m 09s. Therefore, the time at which the measurement is required will occur 00m 50s after that last null.

From Table 3 we note that the time corresponding to 00m 50s is 52,600 microseconds. This means that the beginning of the first (reference) pulse from the above chain will be transmitted 52,600 microseconds after 17h 59m 59s on 15 January.

GERNOT M.R. WINKLER
Director
Time Service Division

***** NO LEAP SECOND DECEMBER 1980 *****

TABLE 1

FIRST TOC FOR EACH DAY
TIMES OF COINCIDENCE (NULL) EPHEMERIS
GREAT LAKES USA (8970) LORAN-C
89,700 MICROSECONDS/PERIOD

DATE 1981	TIME H	M	S	DATE 1981	TIME H	M	S	DATE 1981	TIME H	M	S
JAN 1	0	10	9	FEB 1	0	10	51	MAR 1	0	11	0
2	0	5	21	2	0	6	3	2	0	6	12
3	0	0	33	3	0	1	15	3	0	1	24
4	0	10	42	4	0	11	24	4	0	11	33
5	0	5	54	5	0	6	36	5	0	6	45
6	0	1	6	6	0	1	48	6	0	1	57
7	0	11	15	7	0	11	57	7	0	12	6
8	0	6	27	8	0	7	9	8	0	7	18
9	0	1	39	9	0	2	21	9	0	2	30
10	0	11	48	10	0	12	30	10	0	12	39
11	0	7	0	11	0	7	42	11	0	7	51
12	0	2	12	12	0	2	54	12	0	3	3
13	0	12	21	13	0	13	3	13	0	13	12
14	0	7	33	14	0	8	15	14	0	8	24
15	0	2	45	15	0	3	27	15	0	3	36
16	0	12	54	16	0	13	36	16	0	13	45
17	0	8	6	17	0	8	48	17	0	8	57
18	0	3	18	18	0	4	0	18	0	4	9
19	0	13	27	19	0	14	9	19	0	14	18
20	0	8	39	20	0	9	21	20	0	9	30
21	0	3	51	21	0	4	33	21	0	4	42
22	0	14	0	22	0	14	42	22	0	14	51
23	0	9	12	23	0	9	54	23	0	10	3
24	0	4	24	24	0	5	6	24	0	5	15
25	0	14	33	25	0	0	18	25	0	0	27
26	0	9	45	26	0	10	27	26	0	10	36
27	0	4	57	27	0	5	39	27	0	5	48
28	0	0	9	28	0	0	51	28	0	1	0
29	0	10	18					29	0	11	9
30	0	5	30					30	0	6	21
31	0	0	42					31	0	1	33

***** NO LEAP SECOND DECEMBER 1980 *****

***** NO LEAP SECOND DECEMBER 1980 *****

TABLE 1

FIRST TOC FOR EACH DAY
TIMES OF COINCIDENCE (NULL) EPHEMERIS
GREAT LAKES USA (8970) LORAN-C
89,700 MICROSECONDS/PERIOD

DATE 1981	TIME H	M	S	DATE 1981	TIME H	M	S	DATE 1981	TIME H	M	S
APR 1	0	11	42	MAY 1	0	2	15	JUN 1	0	2	57
2	0	6	54	2	0	12	24	2	0	13	6
3	0	2	6	3	0	7	36	3	0	8	18
4	0	12	15	4	0	2	48	4	0	3	30
5	0	7	27	5	0	12	57	5	0	13	39
6	0	2	39	6	0	8	9	6	0	8	51
7	0	12	48	7	0	3	21	7	0	4	3
8	0	8	0	8	0	13	30	8	0	14	12
9	0	3	12	9	0	8	42	9	0	9	24
10	0	13	21	10	0	3	54	10	0	4	36
11	0	8	33	11	0	14	3	11	0	14	45
12	0	3	45	12	0	9	15	12	0	9	57
13	0	13	54	13	0	4	27	13	0	5	9
14	0	9	6	14	0	14	36	14	0	0	21
15	0	4	18	15	0	9	48	15	0	10	30
16	0	14	27	16	0	5	0	16	0	5	42
17	0	9	39	17	0	0	12	17	0	0	54
18	0	4	51	18	0	10	21	18	0	11	3
19	0	0	3	19	0	5	33	19	0	6	15
20	0	10	12	20	0	0	45	20	0	1	27
21	0	5	24	21	0	10	54	21	0	11	36
22	0	0	36	22	0	6	6	22	0	6	48
23	0	10	45	23	0	1	18	23	0	2	0
24	0	5	57	24	0	11	27	24	0	12	9
25	0	1	9	25	0	6	39	25	0	7	21
26	0	11	18	26	0	1	51	26	0	2	33
27	0	6	30	27	0	12	0	27	0	12	42
28	0	1	42	28	0	7	12	28	0	7	54
29	0	11	51	29	0	2	24	29	0	3	6
30	0	7	3	30	0	12	33	30	0	13	15
				31	0	7	45				

***** NO LEAP SECOND DECEMBER 1980 *****

TABLE 2
INTERPOLATIONS FOR ALL TOC'S IN A DAY
TIMES OF COINCIDENCE (NULL) EPHEMERIS
GREAT LAKES (8970) LORAN-C

89,700 MICROSECONDS/PERIOD

H	M	S
0	0	0
0	14	57
0	29	54
0	44	51
0	59	48
1	14	45
1	29	42
1	44	39
1	59	36
2	14	33
2	29	30
2	44	27
2	59	24
3	14	21
3	29	18
3	44	15
3	59	12
4	14	9
4	29	6
4	44	3
4	59	0
5	13	57
5	28	54
5	43	51
5	58	48
6	13	45
6	28	42
6	43	39
6	58	36
7	13	33
7	28	30
7	43	27
7	58	24
8	13	21
8	28	18
8	43	15
8	58	12
9	13	9
9	28	6
9	43	3
9	58	0
10	12	57
10	27	54
10	42	51
10	57	48
11	12	45
11	27	42
11	42	39
11	57	36
12	12	33
12	27	30
12	42	27
12	57	24
13	12	21
13	27	18
13	42	15
13	57	12
14	12	9
14	27	6
14	42	3
14	57	0
15	11	57
15	26	54
15	41	51
15	56	48
16	11	45
16	26	42
16	41	39
16	56	36
17	11	33
17	26	30
17	41	27
17	56	24
18	11	21
18	26	18
18	41	15
18	56	12
19	11	9
19	26	6
19	41	3
19	56	0
20	10	57
20	25	54
20	40	51
20	55	48
21	10	45
21	25	42
21	40	39
21	55	36
22	10	33
22	25	30
22	40	27
22	55	24
23	10	21
23	25	18
23	40	15
23	55	12

TABLE 3
INTERPOLATIONS FOR ALL SECONDS BETWEEN TOC'S

GREAT LAKES (8970) LORAN-C
89,700 MICROSECONDS/PERIOD

M	S	(US)	M	S	(US)	M	S	(US)	M	S	(US)	M	S	(US)
0	1	76400	0	51	39300	1	41	2200	2	31	54800	3	21	17700
0	2	63100	0	52	26000	1	42	78600	2	32	41500	3	22	4400
0	3	49800	0	53	12700	1	43	65300	2	33	28200	3	23	80800
0	4	36500	0	54	89100	1	44	52000	2	34	14900	3	24	67500
0	5	23200	0	55	75800	1	45	38700	2	35	1600	3	25	54200
0	6	9900	0	56	62500	1	46	25400	2	36	78000	3	26	40900
0	7	86300	0	57	49200	1	47	12100	2	37	64700	3	27	27600
0	8	73000	0	58	35900	1	48	88500	2	38	51400	3	28	14300
0	9	59700	0	59	22600	1	49	75200	2	39	38100	3	29	1000
0	10	46400	1	0	9300	1	50	61900	2	40	24800	3	30	77400
0	11	33100	1	1	85700	1	51	48600	2	41	11500	3	31	64100
0	12	19800	1	2	72400	1	52	35300	2	42	87900	3	32	50800
0	13	6500	1	3	59100	1	53	22000	2	43	74600	3	33	37500
0	14	82900	1	4	45800	1	54	8700	2	44	61300	3	34	24200
0	15	69600	1	5	32500	1	55	85100	2	45	48000	3	35	10900
0	16	56300	1	6	19200	1	56	71800	2	46	34700	3	36	87300
0	17	43000	1	7	5900	1	57	58500	2	47	21400	3	37	74000
0	18	29700	1	8	82300	1	58	45200	2	48	8100	3	38	60700
0	19	16400	1	9	69000	1	59	31900	2	49	84500	3	39	47400
0	20	3100	1	10	55700	2	0	18600	2	50	71200	3	40	34100
0	21	79500	1	11	42400	2	1	5300	2	51	57900	3	41	20800
0	22	66200	1	12	29100	2	2	81700	2	52	44600	3	42	7500
0	23	52900	1	13	15800	2	3	68400	2	53	31300	3	43	83900
0	24	39600	1	14	2500	2	4	55100	2	54	18000	3	44	70600
0	25	26300	1	15	78900	2	5	41800	2	55	4700	3	45	57300
0	26	13000	1	16	65600	2	6	28500	2	56	81100	3	46	44000
0	27	89400	1	17	52300	2	7	15200	2	57	67800	3	47	30700
0	28	76100	1	18	39000	2	8	1900	2	58	54500	3	48	17400
0	29	62800	1	19	25700	2	9	78300	2	59	41200	3	49	4100
0	30	49500	1	20	12400	2	10	65000	3	0	27900	3	50	80500
0	31	36200	1	21	88800	2	11	51700	3	1	14600	3	51	67200
0	32	22900	1	22	75500	2	12	38400	3	2	1300	3	52	53900
0	33	9600	1	23	62200	2	13	25100	3	3	77700	3	53	40600
0	34	86000	1	24	48900	2	14	11800	3	4	64400	3	54	27300
0	35	72700	1	25	35600	2	15	88200	3	5	51100	3	55	14000
0	36	59400	1	26	22300	2	16	74900	3	6	37800	3	56	700
0	37	46100	1	27	9000	2	17	61600	3	7	24500	3	57	77100
0	38	32800	1	28	85400	2	18	48300	3	8	11200	3	58	63800
0	39	19500	1	29	72100	2	19	35000	3	9	87600	3	59	50500
0	40	6200	1	30	58800	2	20	21700	3	10	74300	4	0	37200
0	41	82600	1	31	45500	2	21	8400	3	11	61000	4	1	23900
0	42	69300	1	32	32200	2	22	84800	3	12	47700	4	2	10600
0	43	56000	1	33	18900	2	23	71500	3	13	34400	4	3	87000
0	44	42700	1	34	5600	2	24	58200	3	14	21100	4	4	73700
0	45	29400	1	35	82000	2	25	44900	3	15	7800	4	5	60400
0	46	16100	1	36	68700	2	26	31600	3	16	84200	4	6	47100
0	47	2800	1	37	55400	2	27	18300	3	17	70900	4	7	33800
0	48	79200	1	38	42100	2	28	5000	3	18	57600	4	8	20500
0	49	65900	1	39	28800	2	29	81400	3	19	44300	4	9	7200
0	50	52600	1	40	15500	2	30	68100	3	20	31000	4	10	83600

EXAMPLE -- NOT FOR TIMING

TABLE 3
INTERPOLATIONS FOR ALL SECONDS BETWEEN TOC'S

GREAT LAKES (8970) LORAN-C
89,700 MICROSECONDS/PERIOD

M	S	(US)	M	S	(US)	M	S	(US)	M	S	(US)	M	S	(US)
4	11	70300	5	1	33200	5	51	85800	6	41	48700	7	31	11600
4	12	57000	5	2	19900	5	52	72500	6	42	35400	7	32	88000
4	13	43700	5	3	6600	5	53	59200	6	43	22100	7	33	74700
4	14	30400	5	4	83000	5	54	45900	6	44	8800	7	34	61400
4	15	17100	5	5	69700	5	55	32600	6	45	85200	7	35	48100
4	16	3800	5	6	56400	5	56	19300	6	46	71900	7	36	34800
4	17	90200	5	7	43100	5	57	6000	6	47	58600	7	37	21500
4	18	66900	5	8	29800	5	58	82400	6	48	45300	7	38	8200
4	19	53600	5	9	16500	5	59	69100	6	49	32000	7	39	84600
4	20	40300	5	10	3200	6	0	55800	6	50	18700	7	40	71300
4	21	27000	5	11	79600	6	1	42500	6	51	5400	7	41	58000
4	22	13700	5	12	66300	6	2	29200	6	52	81800	7	42	44700
4	23	400	5	13	53000	6	3	15900	6	53	68500	7	43	31400
4	24	76800	5	14	39700	6	4	2600	6	54	55200	7	44	18100
4	25	63500	5	15	26400	6	5	79000	6	55	41900	7	45	4800
4	26	50200	5	16	13100	6	6	65700	6	56	28600	7	46	81200
4	27	36900	5	17	89500	6	7	52400	6	57	15300	7	47	67900
4	28	23600	5	18	76200	6	8	39100	6	58	2000	7	48	54600
4	29	10300	5	19	62900	6	9	25800	6	59	78400	7	49	41300
4	30	86700	5	20	49600	6	10	12500	7	0	65100	7	50	28000
4	31	73400	5	21	36300	6	11	88900	7	1	51800	7	51	14700
4	32	60100	5	22	23000	6	12	75600	7	2	38500	7	52	1400
4	33	46800	5	23	9700	6	13	62300	7	3	25200	7	53	77800
4	34	33500	5	24	86100	6	14	49000	7	4	11900	7	54	64500
4	35	20200	5	25	72800	6	15	35700	7	5	88300	7	55	51200
4	36	6900	5	26	59500	6	16	22400	7	6	75000	7	56	37900
4	37	83300	5	27	46200	6	17	9100	7	7	61700	7	57	24600
4	38	70000	5	28	32900	6	18	85500	7	8	48400	7	58	11300
4	39	56700	5	29	19600	6	19	72200	7	9	35100	7	59	87700
4	40	43400	5	30	6300	6	20	58900	7	10	21800	8	0	74400
4	41	30100	5	31	82700	6	21	45600	7	11	8500	8	1	61100
4	42	16800	5	32	69400	6	22	32300	7	12	84900	8	2	47800
4	43	3500	5	33	56100	6	23	19000	7	13	71600	8	3	34500
4	44	79900	5	34	42800	6	24	5700	7	14	58300	8	4	21200
4	45	66600	5	35	29500	6	25	82100	7	15	45000	8	5	7900
4	46	53300	5	36	16200	6	26	68800	7	16	31700	8	6	84300
4	47	40000	5	37	2900	6	27	55500	7	17	18400	8	7	71000
4	48	26700	5	38	79300	6	28	42200	7	18	5100	8	8	57700
4	49	13400	5	39	66000	6	29	28900	7	19	81500	8	9	44400
4	50	100	5	40	52700	6	30	15600	7	20	68200	8	10	31100
4	51	76500	5	41	39400	6	31	2300	7	21	54900	8	11	17800
4	52	63200	5	42	26100	6	32	78700	7	22	41600	8	12	4500
4	53	49900	5	43	12800	6	33	65400	7	23	28300	8	13	80900
4	54	36600	5	44	89200	6	34	52100	7	24	15000	8	14	67600
4	55	23300	5	45	75900	6	35	38800	7	25	1700	8	15	54300
4	56	10000	5	46	62600	6	36	25500	7	26	78100	8	16	41000
4	57	86400	5	47	49300	6	37	12200	7	27	64800	8	17	27700
4	58	73100	5	48	36000	6	38	88600	7	28	51500	8	18	14400
4	59	59800	5	49	22700	6	39	75300	7	29	38200	8	19	1100
5	0	46500	5	50	9400	6	40	62000	7	30	24900	8	20	77500

TABLE 3
INTERPOLATIONS FOR ALL SECONDS BETWEEN TOC'S

GREAT LAKES (8970) LORAN-C
89,700 MICROSECONDS/PERIOD

M	S	(US)	M	S	(US)	M	S	(US)	M	S	(US)	M	S	(US)
8	21	64200	9	11	27100	10	1	79700	10	51	42600	11	41	5500
8	22	50900	9	12	13800	10	2	66400	10	52	29300	11	42	81900
8	23	37600	9	13	500	10	3	53100	10	53	16000	11	43	68600
8	24	24300	9	14	76900	10	4	39800	10	54	2700	11	44	55300
8	25	11000	9	15	63600	10	5	26500	10	55	79100	11	45	42000
8	26	87400	9	16	50300	10	6	13200	10	56	65800	11	46	28700
8	27	74100	9	17	37000	10	7	89600	10	57	52500	11	47	15400
8	28	60800	9	18	23700	10	8	76300	10	58	39200	11	48	2100
8	29	47500	9	19	10400	10	9	63000	10	59	25900	11	49	78500
8	30	34200	9	20	86800	10	10	49700	11	0	12600	11	50	65200
8	31	20900	9	21	73500	10	11	36400	11	1	89000	11	51	51900
8	32	7600	9	22	60200	10	12	23100	11	2	75700	11	52	38600
8	33	84000	9	23	46900	10	13	9800	11	3	62400	11	53	25300
8	34	70700	9	24	33600	10	14	86200	11	4	49100	11	54	12000
8	35	57400	9	25	20300	10	15	72900	11	5	35800	11	55	88400
8	36	44100	9	26	7000	10	16	59600	11	6	22500	11	56	75100
8	37	30800	9	27	83400	10	17	46300	11	7	9200	11	57	61800
8	38	17500	9	28	70100	10	18	33000	11	8	85600	11	58	48500
8	39	4200	9	29	56800	10	19	19700	11	9	72300	11	59	35200
8	40	80600	9	30	43500	10	20	6400	11	10	59000	12	0	21900
8	41	67300	9	31	30200	10	21	82800	11	11	45700	12	1	8600
8	42	54000	9	32	16900	10	22	69500	11	12	32400	12	2	85000
8	43	40700	9	33	3600	10	23	56200	11	13	19100	12	3	71700
8	44	27400	9	34	80000	10	24	42900	11	14	5800	12	4	58400
8	45	14100	9	35	66700	10	25	29600	11	15	82200	12	5	45100
8	46	800	9	36	53400	10	26	16300	11	16	68900	12	6	31800
8	47	77200	9	37	40100	10	27	3000	11	17	55600	12	7	18500
8	48	63900	9	38	26800	10	28	79400	11	18	42300	12	8	5200
8	49	50600	9	39	13500	10	29	66100	11	19	29000	12	9	81600
8	50	37300	9	40	200	10	30	52800	11	20	15700	12	10	68300
8	51	24000	9	41	76600	10	31	39500	11	21	2400	12	11	55000
8	52	10700	9	42	63300	10	32	26200	11	22	78800	12	12	41700
8	53	87100	9	43	50000	10	33	12900	11	23	65500	12	13	28400
8	54	73800	9	44	36700	10	34	89300	11	24	52200	12	14	15100
8	55	60500	9	45	23400	10	35	76000	11	25	38900	12	15	1800
8	56	47200	9	46	10100	10	36	62700	11	26	25600	12	16	78200
8	57	33900	9	47	86500	10	37	49400	11	27	12300	12	17	64900
8	58	20600	9	48	73200	10	38	36100	11	28	88700	12	18	51600
8	59	7300	9	49	59900	10	39	22800	11	29	75400	12	19	38300
9	0	83700	9	50	46600	10	40	9500	11	30	62100	12	20	25000
9	1	70400	9	51	33300	10	41	85900	11	31	48800	12	21	11700
9	2	57100	9	52	20000	10	42	72600	11	32	35500	12	22	88100
9	3	43800	9	53	6700	10	43	59300	11	33	22200	12	23	74800
9	4	30500	9	54	83100	10	44	46000	11	34	8900	12	24	61500
9	5	17200	9	55	69800	10	45	32700	11	35	85300	12	25	48200
9	6	3900	9	56	56500	10	46	19400	11	36	72000	12	26	34900
9	7	80300	9	57	43200	10	47	6100	11	37	58700	12	27	21600
9	8	67000	9	58	29900	10	48	82500	11	38	45400	12	28	8300
9	9	53700	9	59	16600	10	49	69200	11	39	32100	12	29	84700
9	10	40400	10	0	3300	10	50	55900	11	40	18800	12	30	71400

TABLE 3
INTERPOLATIONS FOR ALL SECONDS BETWEEN TOC'S

GREAT LAKES (8970) LORAN-C
89,700 MICROSECONDS/PERIOD

M	S	(US)	M	S	(US)	M	S	(US)
12	31	58100	13	21	21000	14	11	73600
12	32	44800	13	22	7700	14	12	60300
12	33	31500	13	23	84100	14	13	47000
12	34	18200	13	24	70800	14	14	33700
12	35	4900	13	25	57500	14	15	20400
12	36	81300	13	26	44200	14	16	7100
12	37	68000	13	27	30900	14	17	83500
12	38	54700	13	28	17600	14	18	70200
12	39	41400	13	29	4300	14	19	56900
12	40	28100	13	30	80700	14	20	43600
12	41	14800	13	31	67400	14	21	30300
12	42	1500	13	32	54100	14	22	17000
12	43	77900	13	33	40800	14	23	3700
12	44	64600	13	34	27500	14	24	80100
12	45	51300	13	35	14200	14	25	66800
12	46	38000	13	36	900	14	26	53500
12	47	24700	13	37	77300	14	27	40200
12	48	11400	13	38	64000	14	28	26900
12	49	87800	13	39	50700	14	29	13600
12	50	74500	13	40	37400	14	30	300
12	51	61200	13	41	24100	14	31	76700
12	52	47900	13	42	10800	14	32	63400
12	53	34600	13	43	87200	14	33	50100
12	54	21300	13	44	73900	14	34	36800
12	55	8000	13	45	60600	14	35	23500
12	56	84400	13	46	47300	14	36	10200
12	57	71100	13	47	34000	14	37	86600
12	58	57800	13	48	20700	14	38	73300
12	59	44500	13	49	7400	14	39	60000
13	0	31200	13	50	83800	14	40	46700
13	1	17900	13	51	70500	14	41	33400
13	2	4600	13	52	57200	14	42	20100
13	3	81000	13	53	43900	14	43	6800
13	4	67700	13	54	30600	14	44	83200
13	5	54400	13	55	17300	14	45	69900
13	6	41100	13	56	4000	14	46	56600
13	7	27800	13	57	80400	14	47	43300
13	8	14500	13	58	67100	14	48	30000
13	9	1200	13	59	53800	14	49	16700
13	10	77600	14	0	40500	14	50	3400
13	11	64300	14	1	27200	14	51	79800
13	12	51000	14	2	13900	14	52	66500
13	13	37700	14	3	600	14	53	53200
13	14	24400	14	4	77000	14	54	39900
13	15	11100	14	5	63700	14	55	26600
13	16	87500	14	6	50400	14	56	13300
13	17	74200	14	7	37100			
13	18	60900	14	8	23800			
13	19	47600	14	9	10500			
13	20	34300	14	10	86900			

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MODEL 2100 LORAN-C TIMING RECEIVER

February 1982, Addendum Number 1

Paragraph 6.4.5.1 should read as follows:

6.4.5.1 When power is first applied or when TEST 3 is executed, two separate RAM tests are performed. The first test checks that portion of the lower 1024 bytes used for temporary storage by the microprocessor during subroutine calls and interrupt processing. If a problem with this portion of memory is detected, the front panel display will be EIXXHELP and all receiver functions will be inoperative. The value of XX can be 01, 10, or 11, indicating which memory integrated circuit on the MPU/MEMORY circuit board is bad. A value of 01 indicates U29, 10 indicates U26, and 11 indicates both. This memory must be repaired before normal receiver operation is possible. If the MPU stack is working, the second RAM test is run. When this test is run, the display will be E1XXYYYY. If the RAM is good, XX will be 00 and YYYY will be 2048. If a problem is detected, YYYY is the decimal address (0000 through 2047) of the first bad memory location. Use the following table to determine the bad integrated circuit:

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February 1982, Addendum Number 2

In most receivers shipped after April 2, 1982, input and output buffers have been added affecting the signals present on the BNC connectors on the rear panel. The following additions and changes apply to those receivers so equipped. To determine if these changes apply to your receiver, remove the top cover. If there is a small printed circuit board mounted on the BNC connectors on the inside surface of the rear panel, this change has been made. If not, these buffers can be added. Please contact Austron, Inc. for details.

In Section 1.3.2, Electrical Specifications, the drive capability of the FIXED and SLEWABLE 1PPS outputs, and the PHASE SHIFTED 1 MHz and 10 MHz outputs has been increased from 1TTL load to one (1) 50 ohm load. These outputs should be terminated by a 50 ohm load at the input being driven. This specification change also applies to Section 1.4.3 Rear Panel, REF 29, REF 31, REF 45, and REF 47.

In Section 1.3.2, Electrical Specifications, the external 1PPS input is still TTL compatible. However, it will now accept 1PPS pulses as high as +15 volts. Input loading is approximately 1.5 k ohms. This specification change also applies to Section 1.4.3, Rear Panel, REF 46.

Section 2.3.2.1 concerns the input impedance of the EXT REF buffer. If the buffer board has been installed, the impedance change should be made on the buffer board, not the MPU/MEMORY board. As shipped from the factory, the input impedance of the EXT REF buffer is approximately 500 ohms. It can be lowered to 50 ohms by shorting across solder gap, W1, on the component side of the buffer board on the rear panel.

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The following items are included with Addendum 2:

1) Schematic, input/output buffers, Austron P/N 12399020,
2) Assembly Drawing, input/output buffers, Austron P/N 10399019,
3) Parts List, input/output buffers, Austron P/N 10399019.

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February 1982, Addendum Number 3

Schematic Corrections (Section 5.0)

1) Figure 5-9, Schematic, Acquire/Track, 12398088,
Connector P1,
Change A0 to BA0
A1 to BA1
A2 to BA2
A3 to BA3
36 to $\overline{R}$
A8 to BA9
$\overline{A}$ to X

Also, delete the connection from U27 pin 16 to U18 pin 4. Show U18 pin 4 connected to +5V.

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February 1982, Addendum Number 4

Section 6.0, MAINTENANCE.

In Table 6-6 page 6-16, omit the signatures for U48 pins 20, 21, 22, and 23. These address lines can be more easily checked using the "kernal" test.

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February 1982, Addendum Number 5

Section 1.3.2 Electrical Specifications.

The description of "EXT REF INPUT (1, 5, 10 MHz)" should read,

EXT REF INPUT (1, 5, 10 MHz)	1, 5, or 10 MHz (internally switch selectable) at 0.5 - 5 VRMS. Reference accuracy must be 5 parts in 10^8 or better for acquisition and tracking.